

**MF11-W/WP
core memory system
maintenance manual**

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7442 4 LINE TO 1 LINE DECODER
7475 4-BIT BISTABLE LATCH
7483 4-BIT BINARY ADDER
7485 4-BIT COMPARATOR
7520 SENSE AMPLIFIER
82S62 9-BIT PARITY GENERATOR AND CHECKER
74121 MONOSTABLE MULTIVIBRATOR
74154 4-LINE TO 16-LINE DECODER

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CHAPTER 1

MF11-W/WP CORE MEMORY

GENERAL DESCRIPTION

1.1 INTRODUCTION

This manual provides the user with the theory of operation and logic diagrams necessary to understand and maintain the MF11-W Core Memory (no parity) or the MF11-WP Core Memory (with parity). The level of discussion assumes that the reader is familiar with the basic digital computer theory. Both general and detailed descriptions of the core memory are included.

Although memory control signals and data pass through the Unibus, it is beyond the scope of this manual to describe the operation of the Unibus itself. A detailed description of the Unibus is presented in the *PDP-11 Peripherals Handbook*.

A complete set of engineering logic drawings are shipped with each core memory. These drawings are bound in a separate volume entitled *MF11-W 32K Core Memory and Control, Engineering Drawings*. The drawings reflect the latest print revisions and correspond to the specific memory shipped to the user.

1.2 GENERAL DESCRIPTION

1.2.1 Introduction

This paragraph provides a physical description and specifications for the memory. The major functional units of the memory are briefly described and the basic memory operations are discussed.

1.2.2 Physical Description

The MF11-W provides 32,768 (32K) 16-bit words; the MF11-WP provides the same number of words but includes byte parity. Chapter 4 describes the differences between the MF11-W and MF11-WP memory. The chart below shows the various option descriptions associated with the 32K memory.

MF11-W	M8294 32K Unibus Timing Module G116 Sense Inhibit Module G236 X-Y Driver H224D Stack Module (16 bits) 7009295 Backplane Assembly
MM11-W Module Set	Includes all modules listed in MF11-W but does not include backplane assembly.
MF11-WP	M8294 32K Unibus Timing Module G116 Sense Inhibit Module G236 X-Y Driver Module H224C Stack Module (18 bits including parity) 7009295 Backplane Assembly M7259 Parity Control Module
MM11-WP Module Set	Includes all modules listed in MF11-WP, except M7259 Parity Control module and does not include backplane assembly.

If a user has a 32K memory system and wishes to add another 32K, he merely specifies the appropriate module set since the existing backplane assembly can hold 64K of memory. The modules are plugged into the slots designated in Figure 1-1.

NOTE

Parity memory cannot be mixed with non-parity memory on the same backplane.

	1	2	3	4	5	6	7	8	9
A	UNIBUS IN	M7259 PARITY							
B									UNIBUS OUT
C	M8294 32K UNIBUS TIMING		G116 SENSE INHIBIT	H224D* MEMORY	G236 X-Y DRIVER	G236 X-Y DRIVER	H224D* MEMORY	G116 SENSE INHIBIT	
D		BLANK							
E									M8294 32K UNIBUS TIMING
F									

* For MF11-WP (parity memory), Memory stock H224C is used. Viewed from backplane.

11-3835

Figure 1-1 Module Utilization Chart

1.2.3 Specifications

The general MF11-W memory specifications are listed in Table 1-1. Refer to Chapter 4 for additional MF11-WP specifications.

Table 1-1 MF11-W Memory Specifications

Type	Magnetic core, read/write, coincident current, random access		
Organization	Planar, 3D, 3-wire		
Capacity	32,768 (32K) words for MM11-W (16-bit word)		
Maximum Access Time and Cycle Time			
	Bus Mode	Cycle Time	Access Time
	DATI	1150 ns	500 ns
	DATIP	500 ns	500 ns
	DATO-DATOB (PAUSE L)	1150 ns	125 ns
	DATO-DATOB (PAUSE H)	680 ns	100 ns
X-Y Current Margins	$\pm 6\%$ @ 0°C , $\pm 7\%$ @ 25°C , $\pm 5\%$ @ 60°C		
Voltage Requirements	$+5\text{ V} \pm 5\%$ with less than 0.2 V ripple $+20\text{ V} \pm 5\%$ with less than $\pm 5\%$ ripple $-5\text{ V} \pm 5\%$ with less than $\pm 5\%$ ripple		
Average Current Requirements			
Stand by	$+5\text{ V}$: 5.5 A, -5 V : 0.64 A $+20\text{ V}$: 0.6 A		
Memory Active	$+5\text{ V}$: 6.1 A, -5 V : 0.74 A $+20\text{ V}$: 3.4 A		
Power Dissipation (Worst Case)	M8294 Control Module ~ 7 W G236 Drive Module ~35 W H224D Stack Module ~40 W G116 Sense Inhibit Module ~40 W Total at Maximum Repetition Rate: 122 W		
Environment			
Ambient Temperature	0° to 60°C (32° to 140°F)		
Relative Humidity	0-90% (non-condensing)		

1.2.4 Functional Description

1.2.4.1 Introduction – The MF11-W/WP Memory is a read/write, random access coincident current, magnetic core type with a maximum cycle time of 1130 ns and a maximum access time of 425 ns. It is organized in a 3D, 3-wire planar configuration. Word length is 16 bits and the memory consists of 32,768 (32K) words.

The memory can be interleaved in 64K increments for faster operation. Interleaving causes consecutive bus addresses to be located within alternate 32K memory blocks.

The major functional units of the memory (Figure 1-2) are briefly described in the following paragraphs.

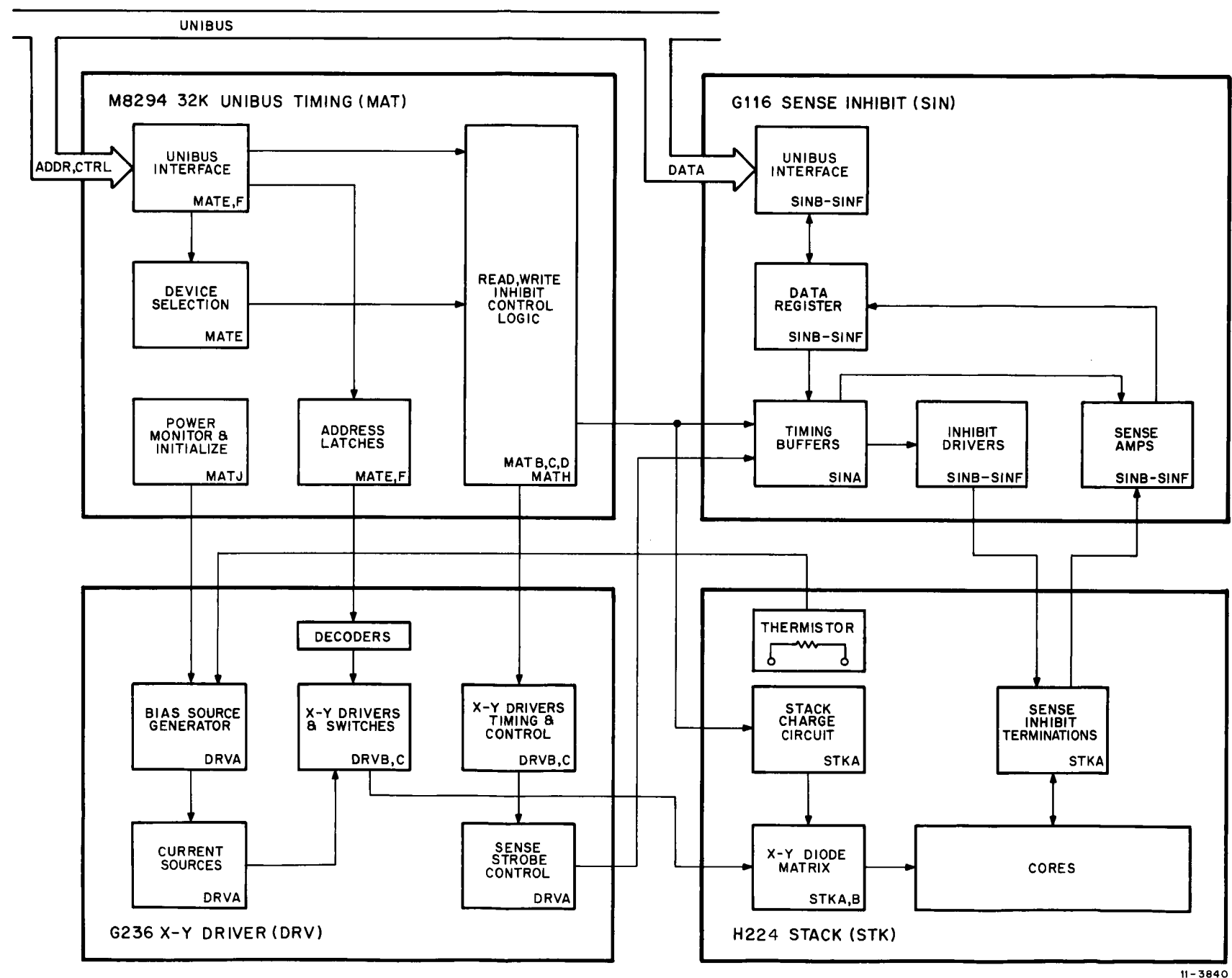


Figure 1-2 MF11-W/WP
Simplified Block Diagram

1.2.4.2 Timing and Control Module – The 32K Unibus Timing module (M8294) contains the control and address portion of the Unibus interface, device selection, power monitor, read-write-inhibit control logic, and the memory address latches.

Unibus Interface – The Unibus interface accepts address and control information from the Unibus. The address information is distributed to the device selector and the address latches. The control signals are supplied to the read, write, and inhibit control logic to initiate the read or write currents in memory. The control signals are BUS C00 and BUS C01 and specify the type of data transfer (DATI, DATIP, DATO, DATOB). If a byte operation (DATOB) is specified, A00L is examined and specifies the appropriate byte.

Device Selection – The device selection logic compares the Unibus address with a prewired jumper configuration. If the address compares, a memory cycle is initiated on the receipt of MSYN. If the address does not compare with the jumper address, the Unibus has addressed some other device and no memory cycle is initiated.

Read-Write-Inhibit Control Logic – The read-write-inhibit control logic operates the timing and control signals to turn on the read, write, and inhibit currents in memory. This is accomplished by propagating a voltage pulse through delay lines and setting and resetting flip-flops as the pulse is propagated through the delay lines. The logic also provides clocking and clearing controls for the data register and controls the time at which the data and SSYN are placed on or taken off the Unibus. In addition, a locking function is provided to lock the address and control information into address latches for use during the memory cycle.

Address Latches – The address latch logic consists of 7475 quad latches (Appendix A) which store the address received from the Unibus for the device selector and stack address decoding circuits. When memory is not busy, the latches are left open and the output merely follows the input. When memory is busy, the output is latched to its previous state. This preserves the address during a memory cycle so that the processor can process other devices without being delayed by the memory.

Power Monitor and Initialize – The power monitor and initialize logic is initiated as a result of BUS INIT or DC LO from the Unibus. Both conditions indicate that further memory operations are to be discontinued. A 3 μ s delay is provided to allow memory to complete the current cycle, then current sources are inhibited until BUS INIT L and DC LO L are removed from the Unibus.

NOTE

The MF11-W/WP incorporates an M8294 32K Unibus Timing module (Chapter 4); other memory systems may employ a different timing and control module although the driver, sense inhibit and stack modules will be the same. Consult the applicable configuration chart in the logic print set.

1.2.4.3 G116 Sense Inhibit Module – The G116 Sense Inhibit module contains the data portion of the Unibus interface, the data register, timing buffers, inhibit drivers, sense amplifiers and threshold circuit.

Unibus Interface – The data portion of the Unibus interface consists of type 8641 Transceivers which apply Unibus data to the data input of the data register and supplies data from the data register to the Unibus (information register). This register is clocked under control of the timing signals from the 32K Unibus Timing module.

Data Register – The data register is a 16-bit flip-flop register used to store the contents of a word after it is destructively read from memory; the same word can then be written back into memory (restored) when in the DATI mode. The register is also used to accept data from the Unibus lines to accommodate the loading of incoming data into the core memory during the DATO or DATOB cycles.

Timing Buffers – The timing buffers are used to buffer the timing signals between the timing and control board and the G116 Sense Inhibit module.

Inhibit Drivers – Each bit mat contains two inhibit/sense lines that pass through all cores on the mat. A bit mat in the MM11-W is a core array of 32,768 cores associated with a particular bit position in all the words in memory. To write a 0 into a selected bit, an inhibit current is passed through the inhibit/sense line that cancels the write current in the Y line. The core does not switch, so it remains in the 0 state. Cores are left in the 0 state at the end of the read portion of the cycle. To write a 1, no inhibit current is passed and the currents in the X and Y lines switch the core to the 1 state.

Sense Amplifiers Threshold – During a read operation, the sense amplifier picks up a voltage induced in the sense/inhibit winding when a core is switched from a 1 to a 0. This signal is detected and amplified by the sense amplifier whose output sets a data register flip-flop to store a 1. In effect, a 1 is read when the core is switched to the 0 state. Cores which were previously set to 0 do not switch and are not affected.

The threshold circuit provides a reference threshold voltage to the sense amplifiers. In a read operation, if the threshold voltage (17 mV) is exceeded during sense strobe time, the sense amplifier produces an output.

1.2.4.4 G236 Driver Module – The G236 Driver module contains the decoders, X and Y drivers and switches, associated timing and control for the X and Y drivers, sense strobe control, bias source generator, and current sources.

Decoders – The decoders decode 15 of the 18 bits on the Unibus address. Eight of these address bits are used for the X address selection – four for X drivers and four for X switches. The remaining seven address bits are used for Y address selection – four for Y switches and three for Y drivers. The three bits not sent to the decoder are used for decoding device selection and byte operation. The decoded X and Y bits specify one core out of 32,768 for each bit of a 16-bit word.

Switches and Drivers – The switches and drivers direct the flow of current through the magnetic cores to ensure the proper polarity for the desired function. This action is necessary because a single X read/write line is used, a single Y read/write line is used, and the current for a write operation is opposite in polarity to the current required for a read operation. There are separate switches and drivers for the read and write circuits in the selection matrix.

Drivers Timing and Control – The drivers timing and control logic receives inputs from the timing and control module and combines the timing signals to derive specific timing pulses and proper timing relationships required by all X-Y drivers and switches as well as current sources.

Sense Strobe Control – The sense strobe control is a one-shot multivibrator whose duration can be controlled by an external voltage input. The control determines when the sense amplifiers are examined.

NOTE

A factory adjustment is made by cutting certain jumpers to determine the optimum position for the sense strobe to occur. Sophisticated test equipment is used in making this factory adjustment; changing the jumper configuration will result in less than optimum memory performance.

Pin AV1 on the G236 Driver module is designated "strobe margin." This pin is normally left open and floats to approximately 2.5 V. However, a voltage can be applied to ensure that the memory has adequate sense strobe margins (ground for early strobe, +5 V for late strobe).

Bias Source Generator – The bias source generator is a dc, temperature compensated, bias current used to control the amplitude of the current from the X and Y current generators and inhibit current sources.

Current Sources – X and Y current generators provide the current necessary to change the state of the magnetic cores. The rise time and amplitude of the output-current waveform have been selected to provide optimum switching of the core states and maximum signal-to-noise ratio for a wide range of temperatures.

1.2.4.5 H224D Stack Module – The H224D Stack module contains the ferrite core array, X–Y diode matrices, sense/inhibit terminations, stack charge circuit, and a thermistor to provide temperature compensation for the bias current.

Ferrite Core Array – The core array is contained in the H224D Stack module and consists of a folded array $256 \times 128 \times 16$ mats, or a total of 524,288 cores.

X–Y Diode Matrix – The X–Y diode matrix is used in conjunction with the drivers and switches and is used to select one of 256 X lines and one of 128 Y lines.

Sense Inhibit Terminations – The sense inhibit terminations terminate the sense inhibit lines in order to minimize transmission line reflections. This is necessary in order that the sense amplifiers can sense core switching with minimum distortion.

Stack Charge Circuit – The stack charge circuit is used to bias the X and Y drive lines to near ground potential during read time, and to near +12 V during write time. The purpose of this is to back-bias the diodes on the X–Y matrix to prevent loss of drive currents due to charging capacitance through unselected diodes.

1.2.5 Basic Memory Operations

The core memory has four basic modes of operation. The main function of the memory is simply to read or write data. Additional modes are provided, however, to allow for byte operation and to postpone the restore cycle in a read-modify-write (DATIP/DATO) cycle. The four basic memory operations are:

1. read/store (DATI)
2. read pause (DATIP)
3. write (DATO)
4. write byte (DATOB)

These four modes are discussed briefly in the following paragraphs.

NOTE

In the following discussions, all operations refer to the master (controlling) device. For example, the term data out indicates data flowing out of the master and into the memory.

1.2.5.1 Data In (DATI) Cycle – The DATI cycle is a read/restore memory cycle. During this operation, the memory reads the information from the selected core location, transfers it to the Unibus, and then writes the information back into the memory location. This last step is necessary because the core memory is a destructive readout device. During the first (read) part of the cycle, the memory strobes the data into a data register and then gates the data to the Unibus. Then, during the second (write) part of the cycle, the memory restores the data back into the addressed memory location.

1.2.5.2 Data In, Pause (DATIP) Cycle – Since the data is destroyed when reading from a particular memory location, it must be restored. However, sometimes it is not desirable to restore the information immediately after reading because the location is to have new data written into it. In this instance, eliminating the restore operation decreases the memory cycle time by approximately 50 percent. The DATIP operation is used for this purpose. The data is read from memory and the restore cycle is inhibited. Because no restore cycle is used, a DATIP must always be directly followed by a write cycle (either DATO or DATOB) on the same address, or data in two addresses will be destroyed.

1.2.5.3 Data Out (DATO) Cycle – The DATO cycle is a write memory cycle used by the master device to transfer data into core memory. To ensure that proper data is stored, the bus data is first clocked into the data register, then the memory location is cleared by reading the cores (thereby setting them all to 0) before writing in the new data. During a normal DATO, the memory first performs the read operation to clear the cores and then performs a write cycle to transfer data from the data register into the selected core location. If a DATO follows a DATIP (rather than a DATI), the sequence is not the same. The DATIP clears core and generates a pause flag; the DATO skips the read cycle and immediately begins the write cycle. This process reduces DATO cycle time by approximately 40 percent. Note that access time is the same (Table 1-1).

1.2.5.4 Data Out, Byte (DATOB) Cycle – The DATOB cycle is similar in function to the DATO cycle, except that during DATOB, data is transferred into the core memory from the bus in byte form rather than as a full word. Actually, an entire word is loaded into the selected memory location: the selected byte, which is new data from the bus; and the non-selected byte, which is restored data from the word previously stored in that memory location. During the read cycle, the non-selected byte is saved by reading it into the dat register while the selected byte is transferred into the data register from the Unibus. During the write cycle, the word is loaded into the memory location from the data register. In effect, the memory is read first and then simultaneously performs a restore cycle for the non-selected byte and a write cycle for the selected byte. The mode can follow a DATIP as described above.

CHAPTER 2

32K UNIBUS TIMING MODULE

2.1 INTRODUCTION

This chapter describes the M8294 32K Unibus Timing module employed with the MF11-W/WP Core Memory system. The chapter is divided into three major sections – memory protection circuits, operation mode selection logic, and control logic. This circuitry is shown on diagram M8294-0-1. Figure 2-1 represents a detailed block diagram of the memory and depicts how the 32K Unibus timing is tied into the core memory system.

2.2 MEMORY PROTECTION CIRCUITS

The memory protection circuits contain the logic to detect BUS INIT L and DC LO L from the Unibus. They also contain the circuitry to detect loss of bias current.

2.2.1 DC LO and BUS INIT

One of the functions of the M8294 32K Unibus Timing module is to detect BUS INIT L and DC LO L from the Unibus. Either signal causes MATJ MSYN HOLDOFF H to be asserted (Figure 2-2). This signal inhibits the initiation of any new memory cycles. A delay circuit consisting of Q1 and Q2 and associated external components (sheet 9 of M8294-0-1) causes MATJ IZ L and MATJ IZ H to be generated after a 3 μ s delay. The IZ signals are used to initialize the 32K Unibus Timing module, while the 3 μ s delay allows the memory to complete any current cycles that were in progress at the time of BUS INIT L or DC LO L. In addition, MATJ IZ L is applied to Q11 on the G236 Driver module, causing Q11 to conduct and Q10 to go to saturation. This inhibits the X-Y current generators (Q1 through Q4 on sheet 4). Transistor Q9 is turned off so that DRVA PWR OK L is no longer asserted. On the G116 Sense Inhibit module, this drives pin 13 of E34 (G116-0-1, sheet 1) high and asserts SINA PF L, which prevents the inhibit drivers (G116-0-1, sheets 2 through 11) from turning on.

NOTE

With DC LO L asserted, the operation occurs as described above even though the +5 V and -5 V power supplies are turned off. The memory protection circuits will operate even if the +20 V power supply is just above +5 V. If the +20 V supply produces less than +5 V, the circuits may not operate properly; this makes no difference, however, as no substantial driver currents are generated.

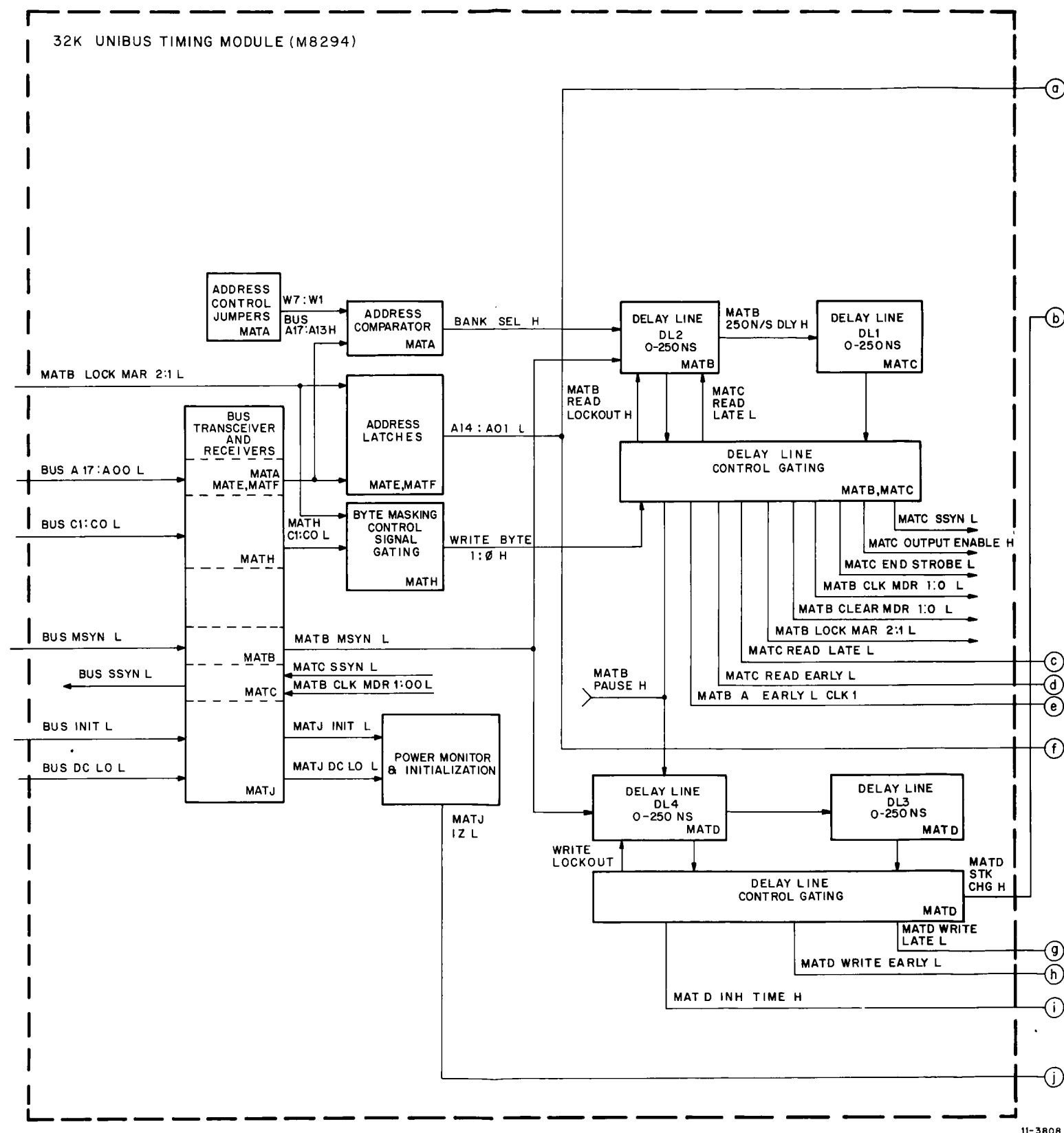


Figure 2-1 MF11-W Detailed
Block Diagram (Sheet 1 of 2)



Table 2-1 Selection of Bus Transaction

X = irrelevant

The logic that decodes the bus operation and byte selection is shown on M8294-0-1, sheet MATH. Bits BUS C01, BUS C00, and BUS A00 are supplied to three receivers from the Unibus. The receivers for BUS C00 and BUS C01 are located on sheet MATH and the receiver for BUS A00 is located on sheet MATF. The BUS C01 and BUS C00 signals are applied to a bistable latch and generate both polarities of MATH C0 and MATH C1. These signals are combined with MATF A00 and generate both polarities of MATH WRITE BYTE (0) and MATH WRITE BYTE (1). These signals in turn, are used to enable the following signals:

MATB	CLK	MDR	0	L
MATB	CLK	MDR	1	L
MATB	CLEAR	MDR	0	L
MATB	CLEAR	MDR	1	L
DRVA	SS0	L		
DRVA	SS1	L		

In addition, MATH C1 L is used to enable MATC OUTPUT ENABLE H. These signals are listed in Table 2-2 which tabulates the memory operating signals generated for each of the bus operations. To avoid confusion in interpreting the transactions listed in Table 2-2, the purpose of the PAUSE flip-flop is discussed briefly. During DATIP, the PAUSE flip-flop is set during the read operation which inhibits the restore (write) operation. The DATIP must be followed by a DATO or DATOB on the same address. The DATO or DATOB that follows a DATIP is shorter than a standard DATO or DATOB because the initial clear operation is eliminated. In Table 2-2, the suffix PAUSE L identifies the standard transactions; the suffix PAUSE H identifies the DATO and DATOB transactions that must follow a DATIP.

2.3.1 Operating Modes

2.3.1.1 Master Sync – In a bus operation, the master device always times the MSYN signal to ensure that MSYN does not reach the slave device prior to the time that the address and control lines on the Unibus have been decoded and are stabilized. Consequently, the bus receiver outputs for the address and control signals indicate the address and mode of the next bus cycle at least 75 ns before BUS MSYN L is received. This 75 ns delay is necessary to allow time for: a) device selection, b) address decoding, and c) mode selection.

2.3.1.2 Slave Synchronization (SSYN) Circuit – Slave synchronization (SSYN) is the response of the slave device to master synchronization (MSYN). The master places address information, mode control information, and data (if a DATO or DATOB is selected) on the Unibus. It then asserts BUS MSYN L only if BUS SSYN L from the previous slave device is cleared, which indicates that the bus transactions can be accomplished. The slave asserts BUS SSYN L when it has data to send (DATI or DATIP) or when it has received data (DATO or DATOB). The master receives BUS SSYN L in either case and clears BUS MSYN L.

When the slave receives the cleared BUS MSYN L, it clears BUS SSYN L, which frees the bus. This brief statement of the SSYN/MSYN interaction is necessary to understand the operation of the memory SSYN circuit. Details of the SSYN/MSYN interaction during all bus transactions can be found in the *PDP-11 Peripherals Handbook*.

2.3.1.3 Device Selection – In order to select the memory, the address lines BUS A17:A01 L must indicate one of the 32K word addresses starting at the minimum address selected by jumpers W7 through W3. The 7485 IC (E34) on M8294-0-1, sheet MATA, examines the received address and compares it with the minimum address configured by jumpers W7 through W3. This address is the initial address in a 32K bank. The output (pin 5) of E34 is asserted if the received address is equal to or greater than the address specified by the jumpers.

Table 2-2 Generation of Memory Operating Signals

Mode	Byte Control A00	Mode Control		State of PAUSE Flip-Flop	Signals Generated							Operational Sequence
		C01	C02		DRVA SS0 L	DRVA SS1 L	MATB CLR MDR (0) L	MATB CLR MDR (1) L	MATB CLK MDR (0) L	MATB CLK MDR (1) L	MATC OUTPUT ENABLE H	
DATI	X	0	0	Reset	✓	✓	✓	✓			✓	Read-restore.
DATIP	X	0	1	Reset-Set	✓	✓	✓	✓			✓	Read-pause. Restore inhibited by PAUSE flip-flop.
DATO PAUSE L	X	1	0	Reset					✓	✓		Clear-write
DATO PAUSE H	X	1	0	Set					✓	✓		Write. Must follow DATIP.
DATOB PAUSE L	0	1	1	Reset		✓		✓	✓			Clear-write selected byte 0. Read-restore nonselected byte 1.
DATOB PAUSE H	0	1	1	Set				✓	✓			Write selected byte 0. Restore non-selected byte 1. Must follow DATIP.
DATOB PAUSE L	1	1	1	Reset	✓		✓				✓	Clear-write selected byte 1. Read-restore nonselected byte 0.
DATOB PAUSE H	1	1	1	Set			✓				✓	Write selected byte 1. Restore non-selected byte 0. Must follow DATIP.

X = irrelevant

The output (pin 7) of the other 7485 IC (E31) is asserted if the received address is less than the jumper address, plus 32K, which means that the address is in the specified bank. If both pin 5 of E34 and pin 7 of E31 are asserted, the device is selected and MATA BANK SEL L is asserted.

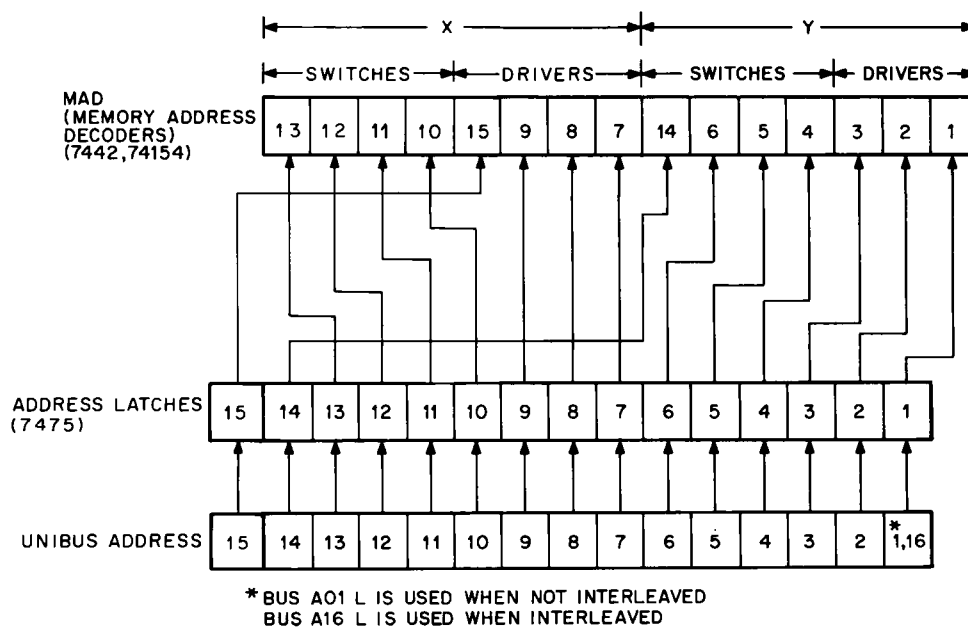
BANK SEL L will also be asserted if the starting address jumpers are cut for 96K or higher and pin 5 of start address comparator E34 is asserted. If interleaving is employed, BANK SEL L will be asserted if the starting address jumpers are cut for 64K or higher and pin 5 of E34 is asserted.

NOTE

BANK SEL L will always be inhibited for bus addresses between 124K and 128K. These addresses are reserved for hardware registers and peripheral devices.

2.3.1.4 Address Decoding – Bus address lines (A15:A01) are received by type 8640 bus receivers (sheets MATA, E, F, and H). The outputs of these receivers feed 7475 quad latches. The outputs of the latches follow the inputs prior to receipt of BUS MSYN L. The outputs of the latches are applied to the 7442 and 74154 memory address decoders on the G236 Driver module (sheets DRVB and DRVC). The decoders decode three or four inputs to 8 or 16 mutually-exclusive outputs to decode the address as shown below.

1. Bits A14, A06, A05 and A04 are applied to a 74154 decoder (E16) to select one pair of Y read/write switches (Figure 2-4).
2. Bits A03, A02 and A01 are applied to a 7442 decoder (E30) to select one pair of Y read/write drivers.
3. Bits A13, A12, A11 and A10 are applied to a 74154 decoder (E25) to select one pair of X read/write switches.
4. Bits A15, A09, A08 and A07 are applied to a 74154 decoder (E39) to select one pair of X read/write drivers.



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Figure 2-4 Switch and Driver Selection

Selection of the appropriate X and Y read/write drivers is accomplished prior to the receipt of BUS MSYN L. The switches and drivers are not turned on, however, until a timing cycle is initiated by BUS MSYN L and MATA BANK SEL H (Paragraph 2.5.2).

2.3.1.5 Mode Selection – The operating mode is determined by BUS C0 L and BUS C1 L. The four operating modes are:

Mode	BUS C0 L	BUS C1 L	Description
DATI	H	H	Read-restore
DATIP	L	H	Read-pause
DATO	H	L	Clear write
DATOB	L	L	Clear (byte)-write (byte)

The DATOB cycle refers to byte operation and performs a clear/write cycle on the byte indicated by BUS A00 L and a read-restore cycle on the other byte.

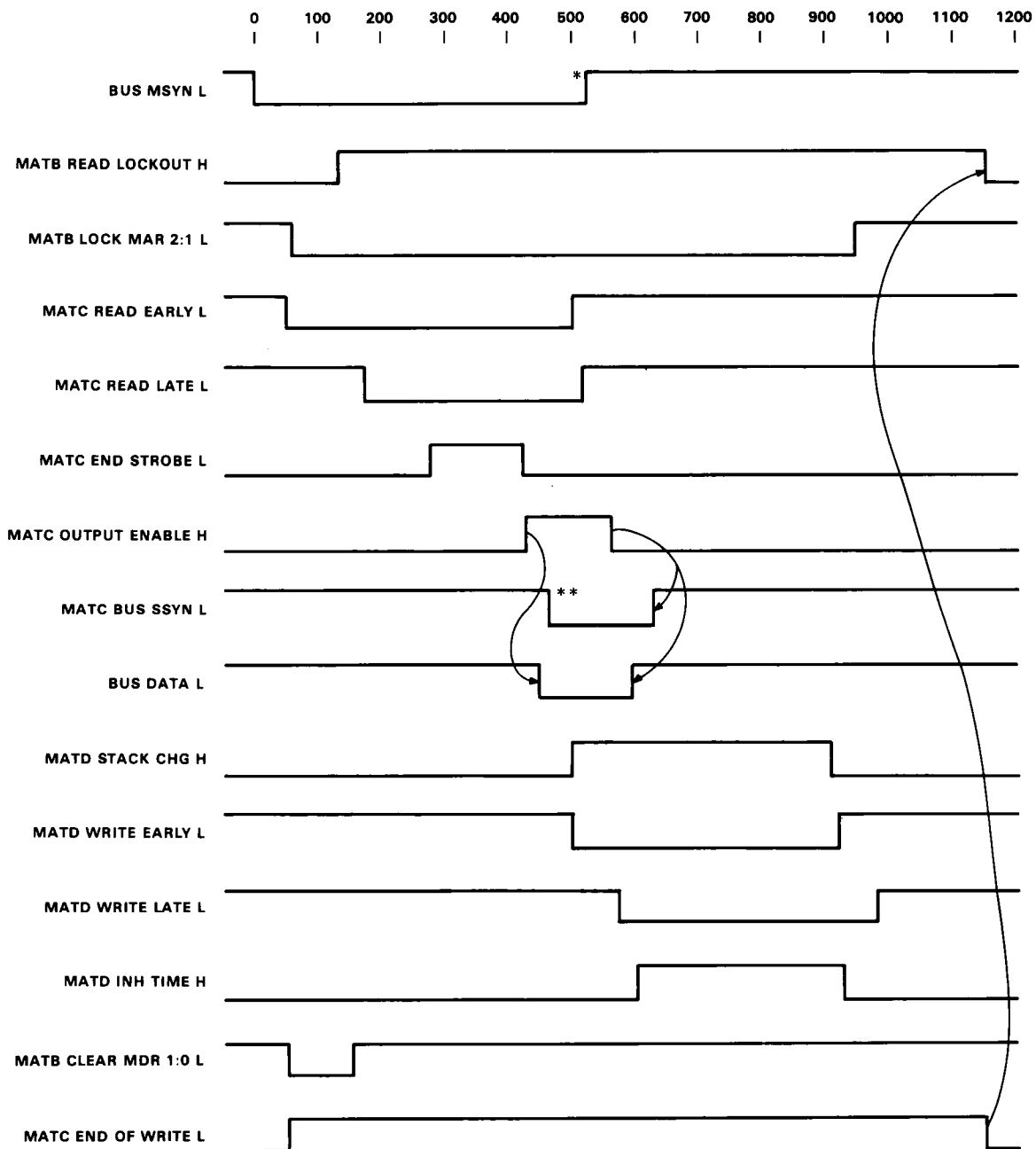
The C0, C1, and A0 signals are treated similar to the address signals (received and stored in 7475 latches). The byte masking logic (on MATH) uses the C00, C01, and A00 signals to generate both polarities of MATH WRITE BYTE 0 and MATH WRITE BYTE 1. These signals are used to indicate whether a clear-write operation or a read-restore operation is to be performed on the respective bytes.

Figure 2-5 shows the timing for the DATI mode, Figure 2-6 shows the timing for the DATIP mode, and Figure 2-7 shows the timing for the DATO or DATOB mode. These timing diagrams, in conjunction with the overall flow diagram of the 32K Unibus Timing module and the detailed flows, should provide the reader with the necessary information to understand and repair the timing module.

2.3.1.6 DATI MODE (Read-Restore) – In this mode, MATH WRITE BYTE 0 H and MATH WRITE BYTE 1 H are not asserted. BUS MSYN L is asserted by the processor or master and generates MATB MSYN H. If the READ LOCKOUT flip-flop is not set and MATA BANK SEL H is asserted, MATB A EARLY L is asserted. This signal is applied to the driver module (G236-0-1, sheet 4) to start X and Y read currents flowing.

In addition, MATB MSYN L is applied to the delay line driver gating (E11 on sheet MATB) and will start a voltage pulse down DL2 if the following conditions are met:

1. MATJ MSYN HOLDOFF H is not asserted (indicating that neither BUS INIT L nor BUS DC LO L is asserted).
2. MATA BANK SEL L is asserted.
3. MATB READ LOCKOUT H is not asserted.



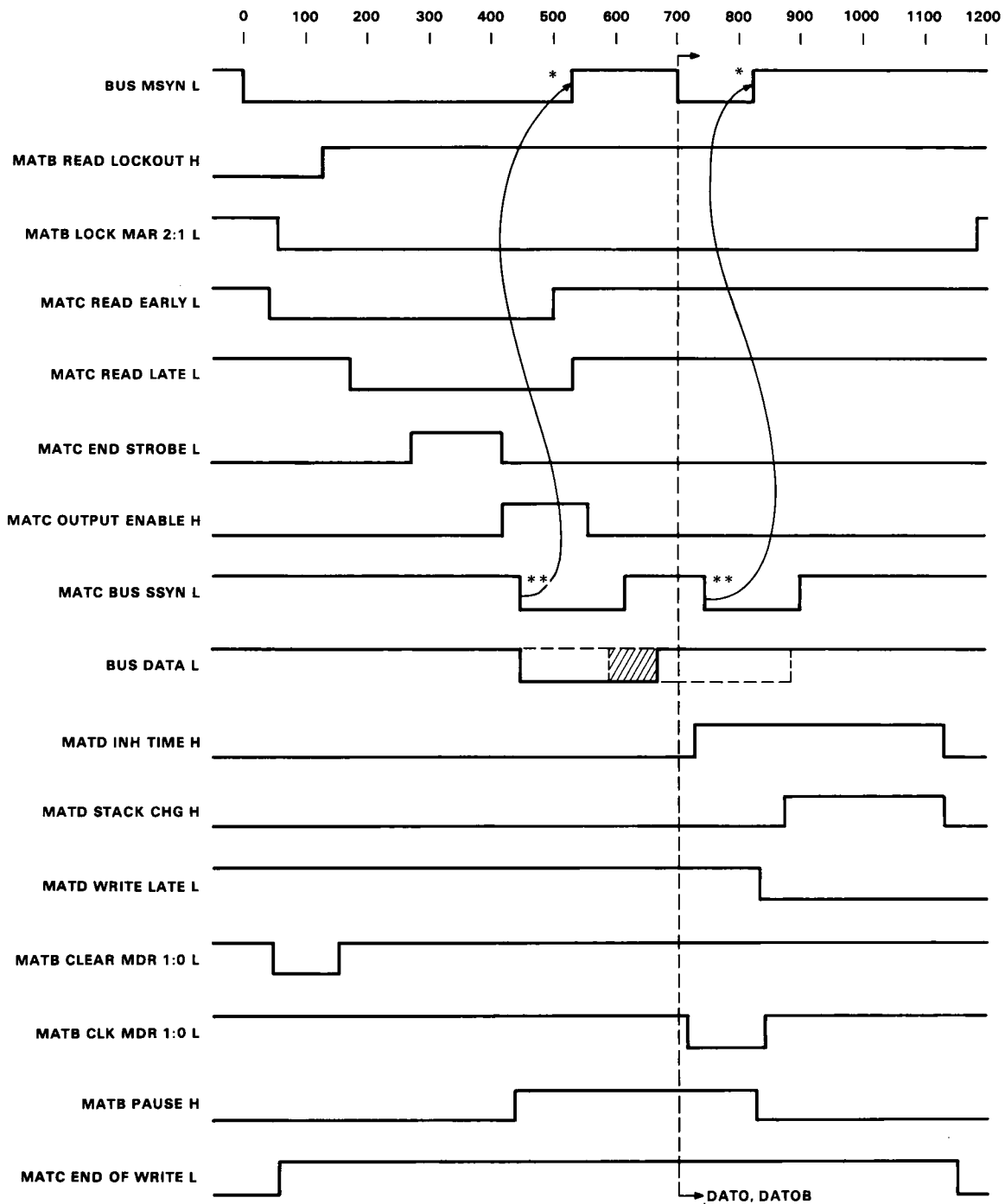
NOTES:

- * Actual time depends on bus and processor delay
- ** In parity systems BUS SSYN L will be 20 μ s later than shown for DATO and DATOB Bus modes.

DATI
BUS C0=H
BUS C1=H

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Figure 2-5 DATI Mode Timing Diagrams

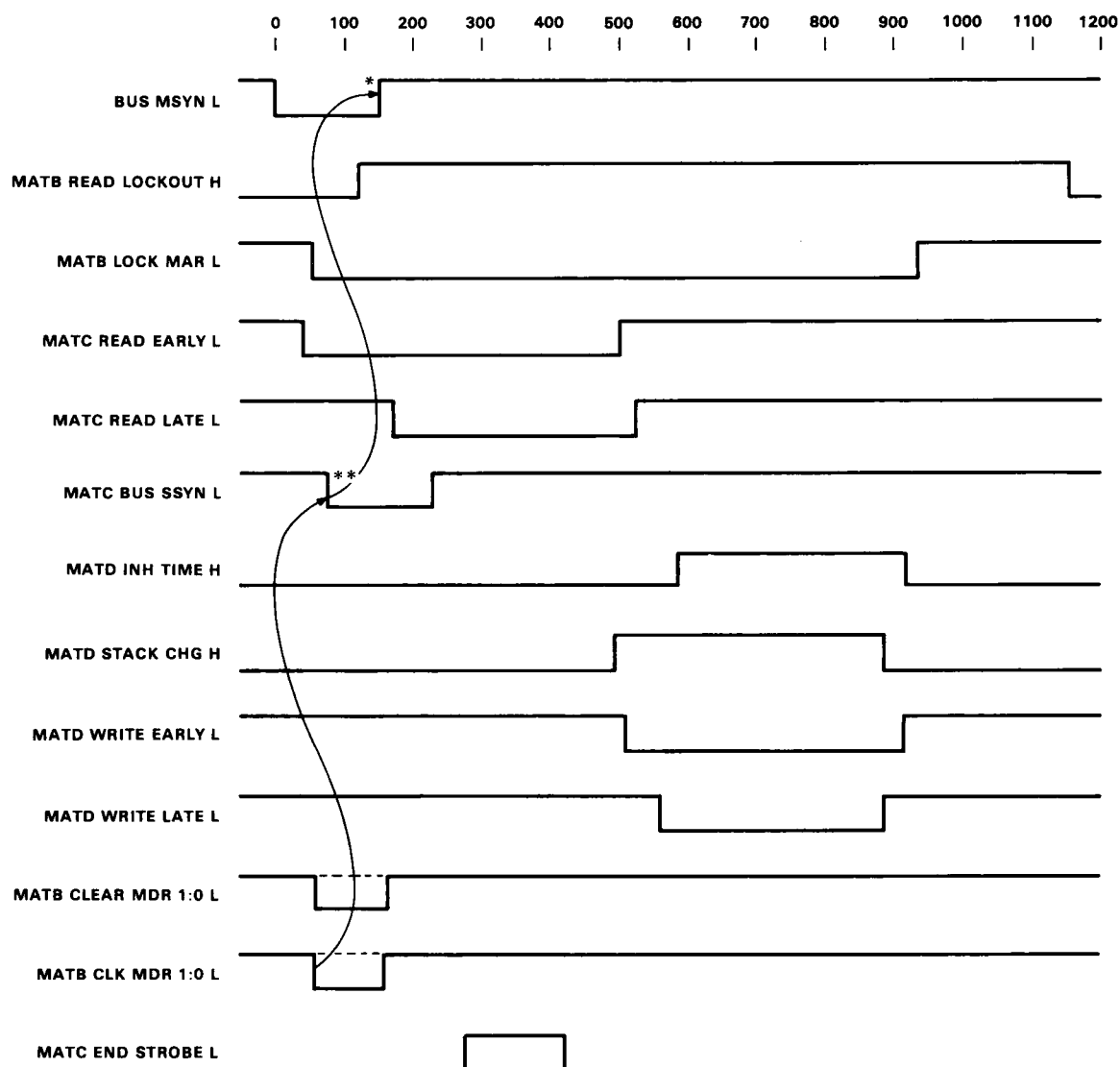


NOTES:
 * Actual time depends on bus and processor delay
 ** In parity systems BUS SSYN L will be 20 μ s later than shown for DATO and DATOB Bus modes.

DATIP	DATO	DATOB
BUS C0=L	BUS C0=H	BUS C0=L
BUS C1=H	BUS C1=L	BUS C1=L
followed by	or	

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Figure 2-6 DATIP Mode Timing Diagrams



NOTES:

* Actual time depends on bus and processor delay

** In parity systems BUS SSYN L will be 20 μ s later than shown for DATO and DATOB Bus modes.

DATO DATOB
 BUS C0=H BUS C0=L
 BUS C1=L BUS C1=L
 or

11-3830

Figure 2-7 DATO, DATOB Mode Timing Diagrams

The voltage pulse going down the delay line will first assert MATB START READ H which does the following:

1. Latches the delay line driver gating on so that the only thing which will turn off the voltage applied to the delay line is the assertion of MATB READ LOCKOUT H.
2. Causes MATB CLEAR MDR 0 L and MATB CLEAR MDR 1 L to be asserted (clears the data register so that new data read from memory can be stored).

3. Causes MATB LOCK MAR 2 L and MATB LOCK MAR 1 L to be asserted (this sets the LOCK MAR flip-flop) which locks the address and control latch outputs to their latest state.
4. Causes the END WRITE flip-flop (on MATD) to be reset (this flip-flop was set by the previous cycle), enabling the READ and WRITE LOCKOUT flip-flops to be set at the appropriate times.
5. Causes MATD MSYN STILL LO L to be asserted. This signal stays asserted until BUS MSYN L goes unasserted.
6. Sets the READ EARLY flip-flop.
7. 125 NS DELAY LINE TAP – sets the READ LATE flip-flop.
8. 75 NS DELAY LINE TAP – sets the READ LOCKOUT flip-flop which turns off the input to the delay line and hence determines the width of the pulse traveling down the delay line.
9. 225 NS DELAY LINE TAP – sets END STROBE flip-flop.
10. 250 NS DELAY LINE TAP – feeds the output of DL2 to the input of DL1.
11. 375 NS DELAY LINE TAP – resets END STROBE flip-flop. Sets the OUTPUT ENABLE flip-flop, allowing data to be gated onto the Unibus. (This flip-flop is reset when BUS MSYN L is cleared.) Resets READ EARLY flip-flop.
12. 450 NS DELAY – the timing signal to turn on the write delay line driver. This starts a voltage pulse down DL4.
13. 425 NS DELAY LINE TAP – causes BUS SSYN to be asserted. (The SSYN flip-flop is reset when BUS MSYN L is cleared.)
14. WRITE 0 DLY H – sets the STACK CHARGE flip-flop which generates MATD WRITE EARLY L. Latches the write delay line driver gating so that only the WRITE LOCKOUT flip-flop can terminate the voltage pulse applied to DL4.
15. WRITE 50 NS DELAY LINE TAP – sets INH flip-flop. Sets WRITE LATE flip-flop.
16. WRITE 75 NS DELAY LINE TAP – sets the WRITE LOCKOUT flip-flop, terminating the voltage pulse traveling down DL4. Sets INHIBIT TIME flip-flop.
17. WRITE 400 NS DELAY LINE TAP – resets STACK CHARGE flip-flop which causes MATD WRITE EARLY L to be unasserted. Resets INHIBIT TIME flip-flop.
18. WRITE 450 NS DELAY LINE TAP – clears the WRITE LATE flip-flop.
19. WRITE 425 NS DELAY LINE TAP – resets the LOCK MAR flip-flop, allowing the latch outputs to once more follow the inputs. Sets the END OF WRITE one-shot and END OF WRITE flip-flop (M8294-0-1, sheet 5). When the one-shot resets, END OF WRITE is asserted. READ and WRITE LOCKOUT flip-flops are reset and a new memory cycle will be initiated upon receipt of BUS MSYN L.

When MATD END OF WRITE L is asserted, the READ and WRITE LOCKOUT flip-flops are reset. This allows a new memory cycle to be initiated upon receipt of a new BUS MSYN L signal.

2.3.1.7 DATIP Mode – The DATIP mode is the same as the DATI mode except that the 400 ns delay line tap sets the PAUSE flip-flop instead of causing a voltage pulse to start down the delay lines. A DATO or DATOB to this memory must follow the DATIP cycle before any other bus cycles.

2.3.1.8 DATO (Clear-Write) – The DATO cycle not preceded by a DATIP cycle (PAUSE flip-flop not set) is the same as the DATI cycle with the following exceptions:

1. MATH WRITE BYTE 0 and MATH WRITE BYTE 1 are both asserted.
2. MATB CLK MDR 0 L and MATB CLK MDR 1 L are asserted instead of MATB CLEAR MDR 0 L and MATB CLEAR MDR 1 L. The clock signals are generated by the assertion of MATH WRITE BYTE 0 and MATH WRITE BYTE 1 and allow the data to be clocked from the Unibus into the data register.
3. BUS SSYN L is asserted by MATB CLOCK MDR 0 L or MATB CLOCK MDR 1 L. The SSYN flip-flop is reset when BUS MSYN L is cleared.

2.3.1.9 DATO – The DATO cycle preceded by a DATIP cycle (PAUSE flip-flop set) is similar to the DATI cycle with the following exceptions:

1. When MATB MSYN H is generated it does not start a pulse down the read delay line since the READ LOCKOUT flip-flop is set.
2. As a result of PAUSE being set, MATB CLK MDR 0 L and MATB CLK MDR 1 L are generated to clock the new bus data into the data register. This also causes BUS SSYN L to be asserted. This signal will drop when BUS MSYN L drops.
3. A voltage pulse is sent down the write delay lines causing the same sequence of events as the write portion of a DATI cycle. This portion of the cycle is initiated by the 300 ns delay line tap in a DATI mode.

2.3.10 DATOB Mode – The DATOB mode is the same as the DATO mode except that A00 indicates the byte selected for the write operation. A read-restore cycle is performed on the non-selected byte. The byte masking logic on sheet MATH WRITE BYTE 0 H or MATH WRITE BYTE 1 H depending on the value of A00.

2.4 DEVICE AND WORD SELECTION

2.4.1 Introduction

When the processor or a peripheral device desires to perform a transaction with the memory, the processor asserts an 18-bit address on Unibus address lines A(17:00). Bits A(15:01) indicate the address of a specific word within the memory. Address bit A00 is used to select the byte (8 bits) transaction when in the DATOB mode.

The memory address is decoded by the device selection circuit on the M8294 32K Unibus Timing module. The word address is stored in a register on this module whose output is decoded to activate the X-Y line switches and drivers that select the addressed word. These circuits contain jumpers that are included or excluded to configure the memory as follows; establish a specific device address; and select interleaved or non-interleaved operation. The device address is a 32K bank, starting on any 4K increment selected by the five device select jumpers.

Table 2-3 lists the function of the address bits (Figure 2-4).

Table 2-3 Addressing Functions

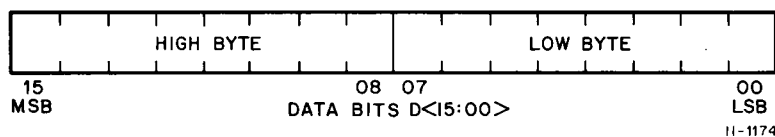
Bus Address	Function
A00	Controls Byte Mode
A01	Non-Interleaved Mode: becomes A01H to M8294 Interleaved Mode: goes to Device Selector
A02, A03, A01H*	Decode Y Drivers
A03, A05, A06, A14	Decode Y Switches
A07, A08, A09, A15	Decode X Drivers
A10, A11, A12, A13	Decode X Switches
A16	Goes to Device Selector Interleaved Mode: becomes A01H to M8294
A13, A14, A15, A17	Goes to Device Selector

*A01H could be a Unibus address bit 1 or 15 depending on the interleaving jumpers.

2.4.2 Memory Organization and Addressing Conventions

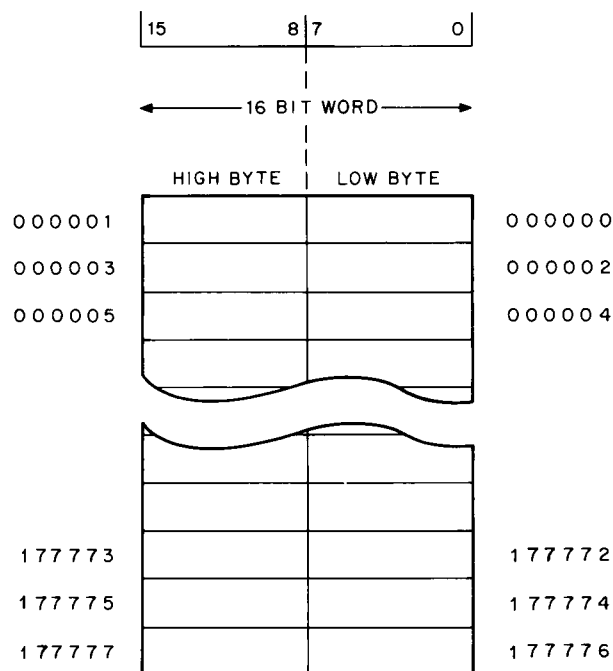
Prior to a detailed discussion of the address selection logic, it is desirable to understand memory organization and addressing conventions.

The memory is organized in 16-bit words, each consisting of two 8-bit bytes. The bytes are identified as low and high as shown below.



Each byte is addressable and has its own address location; low bytes are even numbered and high bytes are odd numbered. Words are addressed at even-numbered locations only; the high (odd) byte is automatically included.

For example, a 32K word memory has 32,768 words or 65,536 bytes; therefore, 65,536 locations are assigned. The address locations are specified as 6-digit octal numbers. The 65,536 locations are designated 000000 through 177777, as shown in Figure 2-8.



11-3801

Figure 2-8 Memory Organization

The address selection logic responds to the binary equivalent of the octal address. The binary equivalent of 017772 is shown below as an example.

ADDRESS BITS A<17:00>																	BIT POSITION	BINARY	OCTAL WORD
17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00		
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0		
0		0		7		7		7		5									

11-1173

Each memory bank requires its own unique device address. For example, assume that a system contains three 32K memory banks as shown in Figure 2-9. The device selector for the 32K non-interleaved memory decodes five address lines [A(17:13)]. Examination of the binary states of these lines for the three memory banks shows that the changes in the states of bits A17 and A16 allow the selection of a unique combination for each bank. The combination, which is the device address, is hardware-selected by jumpers in the device selector.

2.4.3 Device Selector

The device selector is located on the 32K Unibus Timing module. Address bits A01 and A(17:13) are decoded in the device selector to provide the device selection signal MATA BANK SEL L that is used in the control logic. Two combinations of these bits are decoded depending on the memory configuration as shown below.

Memory Configuration	Address Bit
32K Words (non-interleaved)	A(17:13)
32K Words (interleaved)	A01, A(17:13)

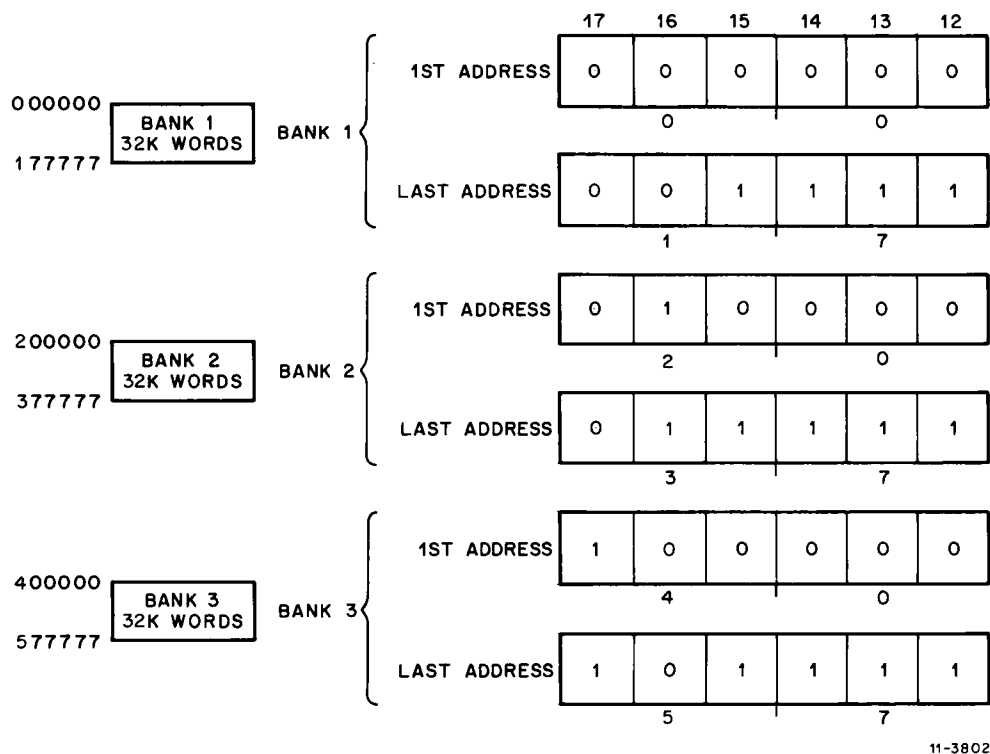


Figure 2-9 Address Assignments for Three Banks of 32K Words Each

Five jumpers (W1, W2, W8, W9, and W10) in the device selection logic on the control module are used to control interleaved or non-interleaved operation of the 32K memory. For non-interleaved operation, W1 is in and W2, W8, W9, and W10 are out. Table 2-4 shows the jumper configuration for non-interleaved memory addresses up to 124K..

Each memory bank must have its own unique device address field. Five jumpers (W3, 4, 5, 6, and 7) in the device selector provide this capability. In drawing M8294-0-1, sheet 2, all the jumpers are shown in place and the device selector would respond only when high signals appear on the Unibus address lines A(17:13). Some jumpers can be removed to allow the device selector to respond to a particular combination of high and low signals on these address lines.

Low signals at the inputs of the 8640 Unibus receivers give highs at their respective outputs. Each receiver output goes to two comparators; one to determine if the bus address is above the minimum address of the field and one to determine if the bus address is below the maximum address of the field (M8294-0-1, sheet MATA).

The other inputs of the 7485 gates associated with bits A(17:13) can be connected to +5 V or ground, depending on whether or not jumpers W3 through W7 are installed. The input is low (ground) with the jumper in; and input is high (+5 V) with the jumper removed.

To configure the jumpers for a specific device address, find the binary equivalent of the assigned octal starting address and insert a jumper in each bit position that contains a 0.

Table 2-5 shows the jumper configuration for interleaved memory addresses up to 124K. When interleaving, two contiguously addressed 32K memory banks must be interleaved.

Table 2-4 Device Address Jumpers (Non-Interleaved)

Memory Bank (Words)	Machine Address (Words) ₈	W3 A17	W4 A16	W5 A15	W6 A14	W7 A13
0-32K	000000-177776	IN	IN	IN	IN	IN
4-36K	020000-217776	IN	IN	IN	IN	OUT
8-40K	040000-237776	IN	IN	IN	OUT	IN
12-44K	060000-257776	IN	IN	IN	OUT	OUT
16-48K	100000-277776	IN	IN	OUT	IN	IN
20-52K	120000-317776	IN	IN	OUT	IN	OUT
24-56K	140000-337776	IN	IN	OUT	OUT	IN
28-60K	160000-357776	IN	IN	OUT	OUT	OUT
32-64K	200000-377776	IN	OUT	IN	IN	IN
36-68K	220000-417776	IN	OUT	IN	IN	OUT
40-72K	240000-437776	IN	OUT	IN	OUT	IN
44-76K	260000-457776	IN	OUT	IN	OUT	OUT
48-80K	300000-477776	IN	OUT	OUT	IN	IN
52-84K	320000-517776	IN	OUT	OUT	IN	OUT
56-88K	340000-537776	IN	OUT	OUT	OUT	IN
60-92K	360000-557776	IN	OUT	OUT	OUT	OUT
64-96K	400000-577776	OUT	IN	IN	IN	IN
68-100K	420000-617776	OUT	IN	IN	IN	OUT
72-104K	440000-637776	OUT	IN	IN	OUT	IN
76-108K	460000-657776	OUT	IN	IN	OUT	OUT
80-112K	500000-677776	OUT	IN	OUT	IN	IN
84-116K	520000-717776	OUT	IN	OUT	IN	OUT
88-120K	540000-737776	OUT	IN	OUT	OUT	IN
92-124K	560000-757776	OUT	IN	OUT	OUT	OUT
96-124K	600000-757776	OUT	OUT	IN	IN	IN
100-124K	620000-757776	OUT	OUT	IN	IN	OUT
104-124K	640000-757776	OUT	OUT	IN	OUT	IN
108-124K	660000-757776	OUT	OUT	IN	OUT	OUT
112-124K	700000-757776	OUT	OUT	OUT	IN	IN
116-124K	720000-757776	OUT	OUT	OUT	IN	OUT
120-124K	740000-757776	OUT	OUT	OUT	OUT	IN

NOTE: The memory may be interleaved in 64K increments, using two contiguously addressed 32K banks.

In the 32K interleaved memory configuration the following changes must be made:

W1 is cut		
W2 is in		
W8 is in		
W9 is in	}	For one 32K of the interleaved pair
W10 is cut		
W9 is cut	}	For the other 32K of the interleaved pair
W10 is in		

Both interleaved memories should be cut for the same starting address.

Table 2-5 Device Address Jumpers (Interleaved)

Memory Bank (Words)	Machine Address (Words) ₈	W3 A17	W4 A16	W5 A15	W6 A14	W7 A13
0-64K	000000-377776	IN	IN	IN	IN	IN
4-68K	020000-417776	IN	IN	IN	IN	OUT
8-72K	040000-437776	IN	IN	IN	OUT	IN
12-76K	060000-457776	IN	IN	IN	OUT	OUT
16-80K	100000-477776	IN	IN	OUT	IN	IN
20-84K	120000-517776	IN	IN	OUT	IN	OUT
24-88K	140000-537776	IN	IN	OUT	OUT	IN
28-92K	160000-557776	IN	IN	OUT	OUT	OUT
32-96K	200000-577776	IN	OUT	IN	IN	IN
36-100K	220000-617776	IN	OUT	IN	IN	OUT
40-104K	240000-637776	IN	OUT	IN	OUT	IN
44-108K	260000-657776	IN	OUT	IN	OUT	OUT
48-112K	300000-677776	IN	OUT	OUT	IN	IN
52-116K	320000-717776	IN	OUT	OUT	IN	OUT
56-120K	340000-737776	IN	OUT	OUT	OUT	IN
60-124K	360000-757776	IN	OUT	OUT	OUT	OUT
64-124K	400000-757776	OUT	IN	IN	IN	IN
68-124K	420000-757776	OUT	IN	IN	IN	OUT
72-124K	440000-757776	OUT	IN	IN	OUT	IN
76-124K	460000-757776	OUT	IN	IN	OUT	OUT
80-124K	500000-757776	OUT	IN	OUT	IN	IN
84-124K	520000-757776	OUT	IN	OUT	IN	OUT
88-124K	540000-757776	OUT	IN	OUT	OUT	IN
92-124K	560000-757776	OUT	IN	OUT	OUT	OUT
96-124K	600000-757776	OUT	OUT	IN	IN	IN
100-124K	620000-757776	OUT	OUT	IN	IN	OUT
104-124K	640000-757776	OUT	OUT	IN	OUT	IN
108-124K	660000-757776	OUT	OUT	IN	OUT	OUT
112-124K	700000-757776	OUT	OUT	OUT	IN	IN
116-124K	720000-757776	OUT	OUT	OUT	IN	OUT
120-124K	740000-757776	OUT	OUT	OUT	OUT	IN

NOTE: If interleaving is desired, the memory must be interleaved in 64K increments, using two contiguously addressed 32K banks.

2.4.4 Word Selection

Word selection requires two levels of decoding. The word address bits are placed in the 14-bit word address register. Outputs from the register are used as inputs to a group of decoders (Figure 2-10). The outputs of the decoders select the proper X and Y read/write switches and drivers.

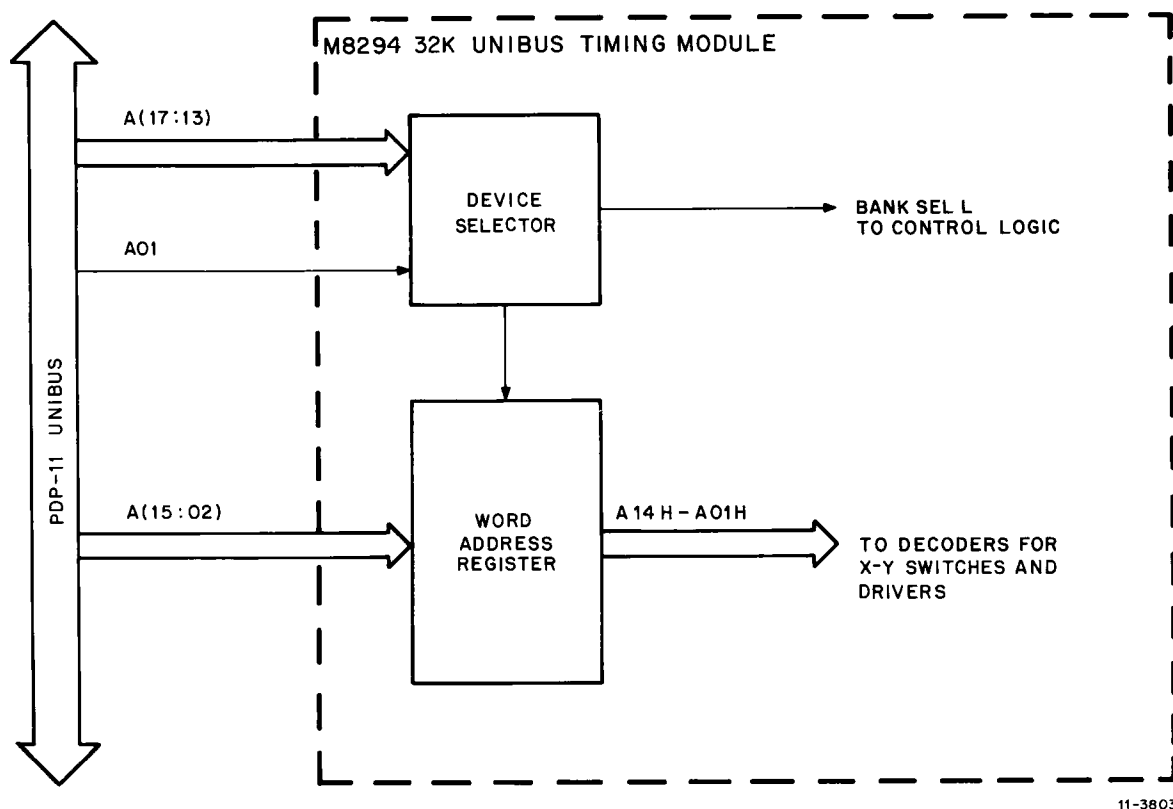


Figure 2-10 Device and Word Address Selection Logic Block Diagram

2.4.4.1 Word Address Register – The word address register is contained on the 32K Unibus timing module. The circuit schematic is shown in drawing M8294-0-1. The register is composed of 4 quad 7475 D-type latches. They are identified as E17, E22, E26, and E38. The word address register cannot be directly cleared or preset; its output responds only to the signal at its D (data) input. Address bits A(14:02) are picked off the Unibus via type 8640 quad receivers. The receiver outputs are applied to the corresponding latch inputs. The latch associated with bit A01 receives its input from the device selector (sheet MATA). The input signal is MATA LEAST BIT H, which is obtained from bit A01 Unibus receiver for a 32K non-interleaved memory. For a 32K interleaved memory, MATA LEAST BIT H is obtained from bit A16 Unibus receiver.

The register latches are locked by MATB LOCK MAR 1 L and MATB LOCK MAR 2 L from the control logic (drawing M8294-0-1, sheet MATB). The generation and timing of this lock signal is discussed in Paragraph 2.5.2. The outputs of the latches are sent to the 7442 and 74154 X-Y line decoders on the driver module (G236-0-1, sheets 1, 2, and 3).

Prior to the generation of the MATB LOCK MAR 1 L and MATB LOCK MAR 2 L, the address lines at the outputs of the latches follow the state of the bus receiver outputs. In this way, the decoder outputs (E16, 25, 30, and 39 on the G236 Driver module) indicate the selected address slightly before BUS MSYN is received. Hence, the X and Y drivers on the G236 module (G236-0-1, sheets 1, 2, and 3) are turned on after receipt of BUS MSYN.

2.5 CONTROL LOGIC

2.5.1 Introduction

The control logic generates the precisely timed signals that initiate, control, and stop the memory operations that are requested as a result of the decoding of the bus transaction. The heart of the control logic is the delay line timing circuit (M8294-0-1, sheet MATB). For better understanding, the read and write memory sequences are described separately with associated timing diagrams. The discussion is to detailed logic level but the signals are not traced through each component. The text is referenced to logic drawing M8294-0-1.

2.5.2 Timing Circuit

The heart of the memory control logic is the timing circuit. When activated, it generates a series of precisely timed signals that control memory operation. The major components of the timing circuit are delay lines (DL1 to DL4) with multiple 25 ns taps (drawing M8294-0-1). The delay line outputs set and reset flip-flops to produce the control signals shown in Figures 2-11 and 2-12.

When the system is turned on, the processor asserts BUS INIT L on the Unibus. This initializing signal is received and eventually asserts MATJ IZ L and MATJ IZ H, as discussed in Paragraph 2.2.1. MATJ IZ L and MATJ IZ H initialize all required flip-flops in the memory and when BUS INIT L is removed, the memory is ready to accept address, control, and data. When the processor asserts BUS MSYN L, a memory cycle is begun (provided the memory is not busy as indicated by MATB READ LOCKOUT H, provided the address is within the device selection limits as indicated by MATA BANK SEL L, and provided DC LO L or BUS INIT L is not asserted). AND-OR-INVERT gate E11 (sheet MATB, zone B-7) on the M8294 module determines if a memory cycle is to occur when BUS MSYN L is received. The output of E11 (Pin 8) is buffered by transistor Q3 which drives a tapped delay line DL2. The pulse width of the signal applied to the delay line is determined by setting the READ LOCKOUT flip-flop at the 75 ns tap of the delay line. Hence, an approximately 100 ns wide positive pulse travels down the 250 ns (tapped every 25 ns) delay line DL2, and then into an identical delay line DL1 (sheet MATC). The leading edge of this pulse traveling down delay lines DL2 and DL1 first sets and then resets flip-flops, generating the timing pulses shown in Figure 2-11 (read cycle). A similar pair of delay lines (DL4 and DL3 – sheet MATD) are used to generate the timing and control signals shown in Figure 2-12 (write cycle). These timing signals are briefly described in the following paragraphs.

2.5.3 MATB START READ H Signal

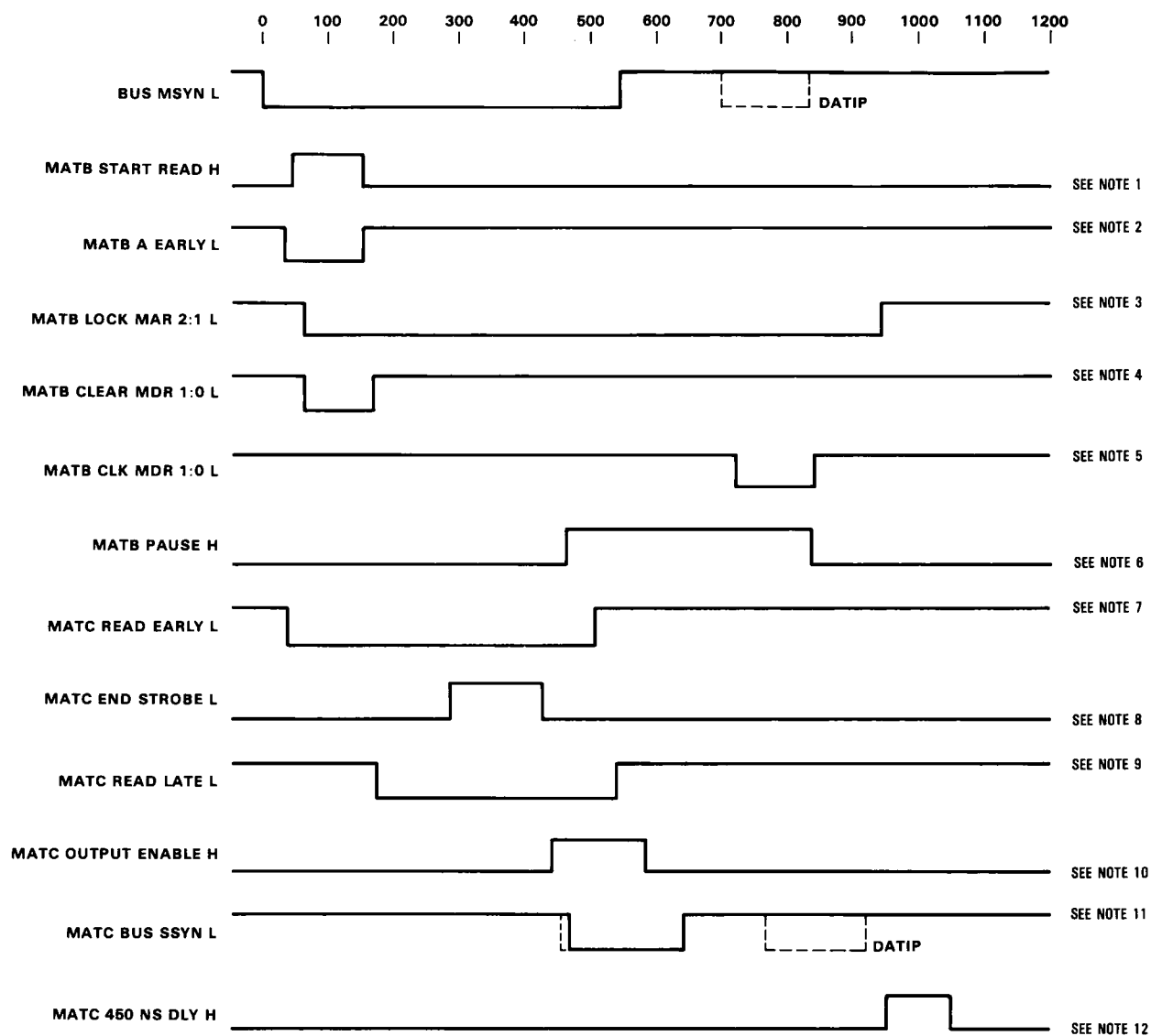
This is the buffered output of transistor Q3 (zone B-6) and is the input to the read delay line DL2. MATB START READ H is 100 ns wide and occurs at the beginning of every read or clear operation. All operations from the bus (except a DATO or DATOB after a DATIP) cause this signal to be asserted.

2.5.4 MATB A EARLY L Signal

The combination of MATA BANK SEL H, MATB MSYN H, and the fact that the memory is not busy causes MATB A EARLY L to be asserted. This is advance timing to inform the G236 Driver module to turn on the Y read current generator, Y read driver, Y read switch, X read current generator and X read switch. The X read driver is not turned on at this time and waits for MATB READ LATE L. MATB A EARLY L is only 100 ns wide, but is closely followed by MATC READ EARLY L which is ORed with MATB A EARLY L on the G236 Driver module.

2.5.5 MATB LOCK MAR 1 L, MATB LOCK MAR 2 L Signals

These signals are asserted when MATB START READ L is asserted. MATB START READ L sets the LOCK MAR flip-flop. This flip-flop is reset near the end of the write cycle by MATD 400 NS DLY L. At this time, the address is no longer needed. When not asserted, the MATB LOCK MAR 1 L and MATB LOCK MAR 2 L signals allow the output of the address latches to follow the inputs to the latches from the bus receivers. The address latches are located on sheets MATE, MATF, and MATH.

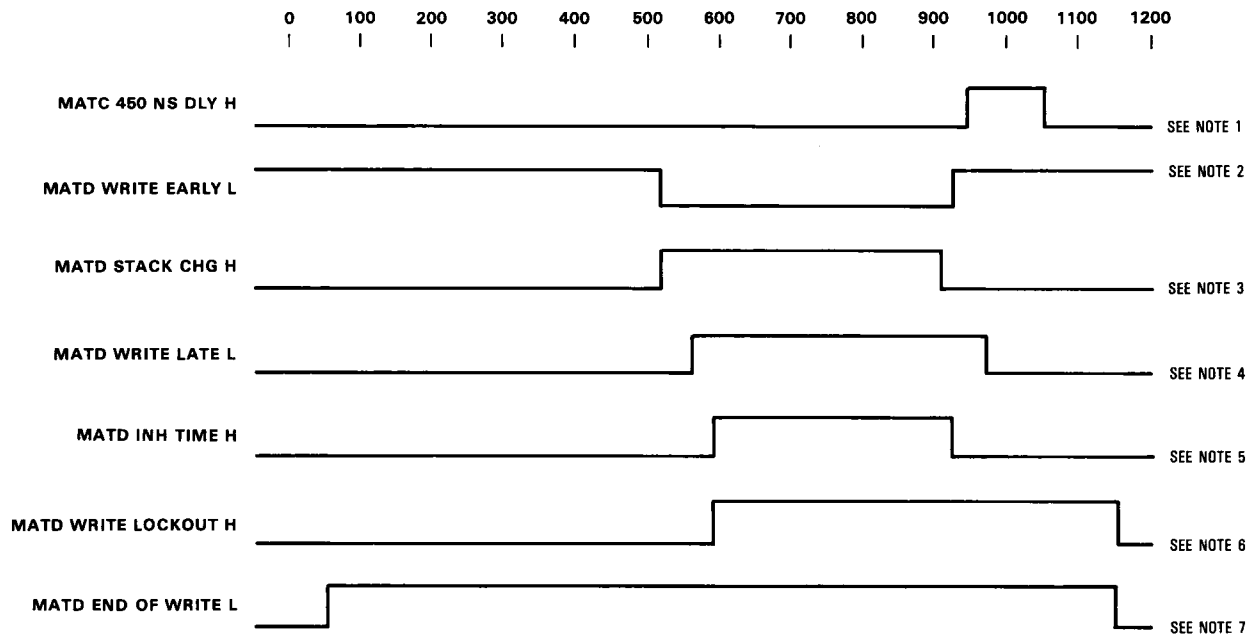


NOTES:

- | | |
|--|---|
| 1 PROVIDES BASIC TIMING FOR ALL MEMORY OPERATIONS AS IT PROPAGATES THROUGH DELAY LINES | 7 CONTROLS READ CURRENT TIMING |
| 2 STARTS READ CURRENTS IN STACK | 8 THE TRAILING EDGE OF THIS SIGNAL ENDS THE SENSE STROBE SIGNALS |
| 3 LOCK THE ADDRESS AND CONTROL REGISTER | 9 OTHER TIMING FOR READ CURRENTS |
| 4 CLEARS DATA REGISTER FOR DATI OR DATIP AND FOR UNSELECTED BYTE IN DATOB | 10 ENABLES DATA BUS DRIVERS ON A DATI OR DATIP |
| 5 CLOCKS NEW DATA INTO DATA REGISTER FOR DATO AND SELECTED BYTE FOR DATOB | 11 INDICATES DATA TAKEN FROM BUS (DATO, DATOB) OR DATA ON BUS (DATI, DATIP) |
| 6 IS SET DURING READ FOR DATIP ONLY | 12 INPUT TO WRITE TIMING CONTROL, WILL INITIATE A WRITE TIMING SEQUENCE UNLESS MATC DATIP CYCLE L IS ASSERTED |

11-3831

Figure 2-11 Read Timing Sequence



NOTES:

- 1 INITIATES WRITE SEQUENCE IN DATO, DATOB OR DATI
- 2 WRITE CURRENT TIMING
- 3 CHARGES STACK
- 4 WRITE CURRENT TIMING
- 5 INHIBIT CURRENT TIMING
- 6 SET WIDTH OF PULSES TRAVELLING DOWN DELAY LINES
- 7 SIGNALS END OF MEMORY CYCLE. RESETS READ AND WRITE LOCKOUT FLIP-FLOPS

11-3832

Figure 2-12 Write Timing Sequence

The outputs of the address latches are fed to the G236 Driver module where they are decoded prior to the receipt of BUS MSYN L. When MATB LOCK MAR 1 L and MATB LOCK MAR 2 L are asserted, the address latches are locked in their present states and cannot follow the outputs from the bus receivers until the signals go unasserted.

2.5.6 MATB CLEAR MDR 0 L, MATB CLEAR MDR 1 L Signals

MATB CLEAR MDR 0 L clears the data register for the low byte (byte 0) immediately preceding the generation of SINA SENSE STROBE 0 H on the G116 Sense Inhibit module. SINA SENSE STROBE 0 H is associated with reading in a DATI, DATIP, or is associated with the unselected byte of a DATOB. In a DATOB, a read-restore cycle is performed on the unselected byte and a clear-write is performed on the selected byte. MATB CLEAR MDR 1 L performs a similar operation for the high byte (byte 1). Both signals are enabled by MATB START READ H. If MATH WRITE BYTE 1 L is enabled, MATB CLEAR MDR 1 L is generated.

2.5.7 MATB CLK MDR 0 L, MATB CLK MDR 1 L Signals

MATB CLK MDR 0 L transfers the bus data receiver outputs into the memory data register associated with byte 0. MATB CLK MDR 1 L transfers the bus data receiver outputs into the memory data register associated with byte 1. The transfer takes place at the beginning of a DATO or DATOB (from the selected byte only), regardless of the state of the PAUSE flip-flop. MATD MSYN STILL LO L prevents the data register from being clocked at the end of a DATIP cycle. When this signal is asserted and PAUSE is set, it means that the BUS MSYN L signal from the Unibus is the MSYN due to the DATIP and has not been removed by the processor.

When MSYN L is released by the processor, MATD MSYN STILL LO L goes unasserted. When the next BUS MSYN L is received (with the PAUSE flip-flop set), the data register can be clocked, for it is known to be the correct MSYN signal. After the DATIP operation, the address and control latches are left in a locked state. Since a DATO or DATOB cycle must follow the DATIP, it is necessary for MATH WRITE BYTE 0 H and MATH WRITE BYTE 1 H to reflect the new control signals (C00, C01, and A00) rather than the signals locked in the latches at the beginning of the DATIP. Consequently, when the PAUSE flip-flop is set, MATB PAUSE H allows the outputs of the bus receivers (sheet MATH) to designate the type of bus operation and the high or low byte. The outputs of the bus receivers accomplish this by modifying MATH WRITE BYTE 0 H and MATH WRITE BYTE 1 H. If PAUSE is not asserted, the outputs of the address and control latches determine the type of bus operation.

2.5.8 MATB PAUSE H Signal

When MATB PAUSE H is asserted, a DATO or DATOB operation is performed in about two-thirds the time normally required. This savings in time results from the fact that the clear operation has already been performed in the DATIP portion of the cycle, and does not have to be repeated for the DATO or DATOB. MATB PAUSE H also allows MATB MSYN H to start the write sequence timing chain. This signal is generated during a DATIP operation by MATC DEL DATIP L and is reset by MATD 75 NS DLY L from the write sequence timing.

2.5.9 MATC READ EARLY L Signal

MATC READ EARLY L and MATB A EARLY L are ORed together (G236-0-1, sheet 2). MATB A EARLY L, when asserted, turns on the X and Y switches and Y drivers. The X drivers are not yet turned on as these drivers are what actually switch the cores. MATB A EARLY L is generated prior to MATC READ EARLY L and turns on the appropriate switches and drivers prior to READ EARLY L time. The reason for this is to allow the transients to occur as long as possible before the cores are switched. When MATC READ EARLY L is unasserted, it turns off the X and Y read drivers.

2.5.10 MATC END STROBE L Signal

MATC END STROBE L controls the trailing edge of the strobe signals by generating DRVA SS0 and DRAV SS1 (G236-0-1, sheet 4, zone B-6). These signals (SS0 and SS1) generate the four strobe signals SINA SENSE STROBE 0, 1, 2, 3 (G116-0-1, sheet 1). The leading edge of the strobe signal are variable and are determined by a one-shot E3 (G236-0-1, sheet 4) which is triggered by DRVC X READ SINK TIME L. The one-shot time delay is controlled by Q6 which may be altered by STROBE MARGIN.

This signal is varied by either grounding AV1 (STROBE MARGIN) on the G236 module or connecting it to +5 V. This moves the leading edge of SINA SENSE STROBES, but does not affect the trailing edge. The sense strobe signals are wide in the MM11-W Memory to allow additional time for the core outputs to be propagated along the extremely long sense lines and to propagate through the associated signal path delays.

2.5.11 MATC READ LATE L Signal

MATC READ LATE L, when asserted, turns on the read X drivers which cause the read X current to start flowing. When the signal goes unasserted, the X and Y read switches are turned off.

2.5.12 MATC OUTPUT ENABLE H Signal

MATC OUTPUT ENABLE H allows the bus drivers located on the G116 module to apply the output data to the UNIBUS on a DATI or DATIP operation. MATC OUTPUT ENABLE H is generated at the same time SENSE STROBE is ended and becomes unasserted when BUS MSYN L becomes unasserted. The OUTPUT ENABLE flip-flop may also be reset by PCL MSYN DISABLE L (not presently utilized).

2.5.13 BUS SSYN L Signal

During a DATO or DATOB, BUS SSYN L is asserted by MATB CLK MDR 0 L or MATB CLK MDR 1 L, or during a DATI or DATIP operation by MATC 400 NS DLY H, which occurs about 25 ns after MATC OUTPUT ENABLE H. When OUTPUT ENABLE H goes unasserted, BUS SSYN L and the data are removed from the bus.

2.5.14 MATC 450 NS DLY H Signal

MATC 450 NS DLY H is an input to the write timing control which starts the write sequence (sheet MATD) unless a DATIP MODE is selected. MATC 450 NS DLY H is generated by the tap on pin 11 of delay line DL1.

2.5.15 MATD WRITE EARLY L Signal

MATD WRITE EARLY L is asserted by E10 (pin 8) at the beginning of the WRITE sequence and is unasserted by a timing signal from pin 7 of DL3 (approximately 375 ns later). MATD WRITE EARLY L turns on the X and Y write current generators and X and Y switches on the G236 module (sheets DRVC and DRVA). It also turns off the same current generators and switches when it becomes unasserted.

2.5.16 MATD STACK CHG H Signal

MATD STACK CHG H is the complement of MATD WRITE EARLY L and is used as the input to the H224 stack charge circuit to reverse bias the unselected X and Y drive matrix diodes.

2.5.17 MATD WRITE LATE L Signal

MATD WRITE LATE L is the same as the MATD WRITE EARLY L signals but is delayed by 50 ns. It controls the turning on and off of the X and Y write drivers (sheets DRVC and DRVA).

2.5.18 MATD INH TIME H Signal

MATD INH TIME H is generated during the write timing sequence. Its function is to provide timing for turning on the INHIBIT drivers.

2.5.19 WRITE LOCKOUT H Signal

The WRITE lockout flip-flop (sheet MATD) prevents bus activity from causing spurious write pulses. It is set by the 75 ns tap of DL4 and reset by MATD END OF WRITE L.

2.5.20 MATD END OF WRITE L Signal

The END WRITE flip-flop is set at the end of a write sequence. The output of the END WRITE flip-flop is combined with MATC SSYN L. As soon as SSYN becomes unasserted, which means that MSYN and SSYN have gone away, END OF WRITE L is asserted which indicates completion of the memory cycle. The END OF WRITE L signal resets the read and write lockout flip-flops at the end of a write sequence.



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CHAPTER 3

DRIVER, SENSE AND STACK MODULES

3.1 INTRODUCTION

This chapter provides a detailed description of the MM11-W Memory. The detailed description covers the core array, switches and drivers, current generation, stack discharge circuitry, and sense/inhibit circuitry.

3.2 CORE ARRAY

The ferrite core memory consists of 16 memory mats (18 for MF11-WP) arranged in a planar configuration. Each mat contains 32,768 ferrite cores arranged in a 128×256 array. Each mat represents a single bit position of a word. This planar configuration provides a total of 32,768 16-bit word locations (18 for MF11-WP). Each ferrite core can assume a stable magnetic state corresponding to either a binary 1 or a binary 0. Even if power is removed from the core, the core retains its state until changed by appropriate control signals. The outside diameter of each core is 18 mil; the inside diameter is approximately 11 mil. Each core is 4.5 mil thick.

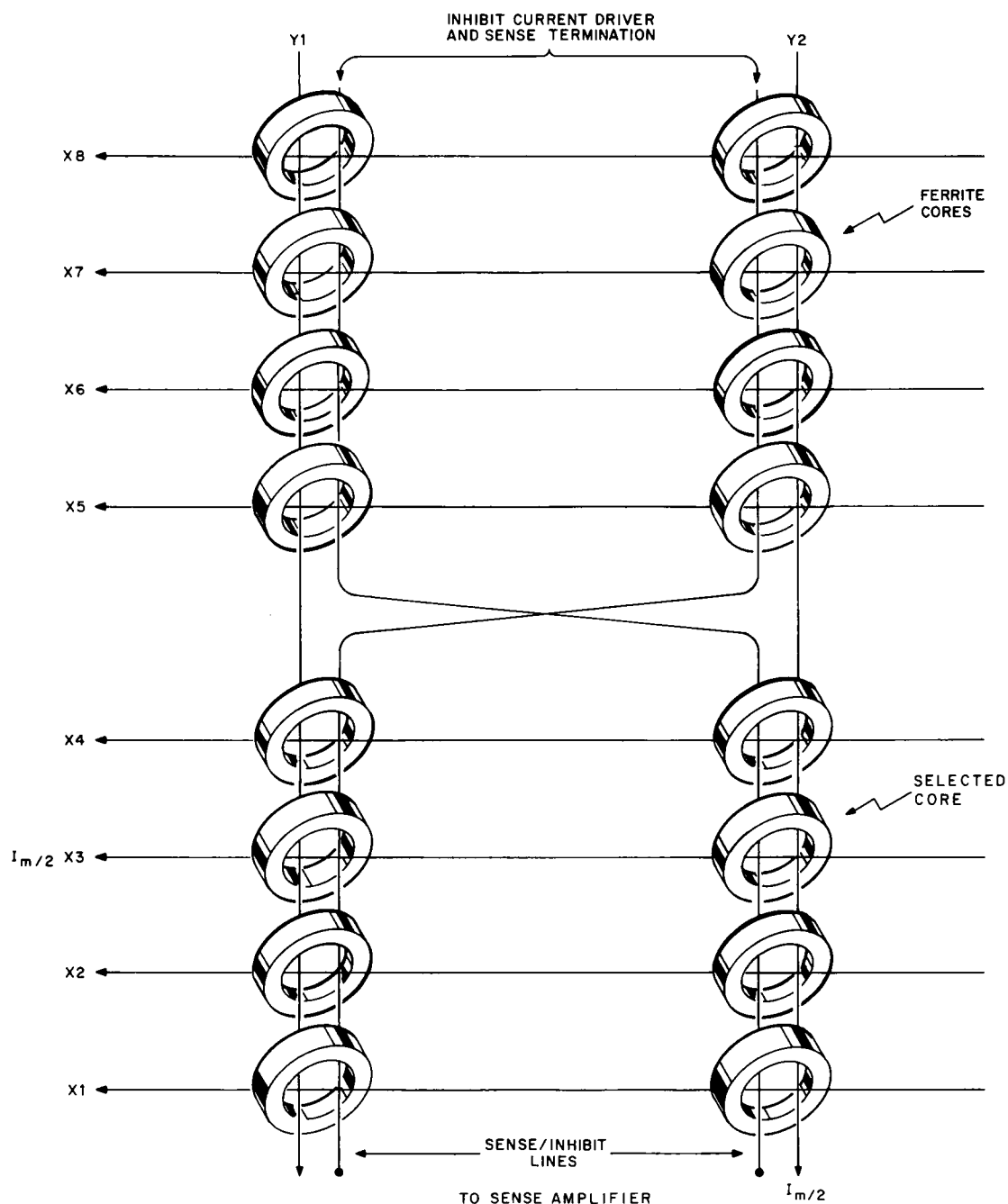
Each core is threaded by three wires, providing means for selection and core switching. Each X axis read/write winding passes through all cores in a horizontal row for all 16 or 18 mats. Each Y axis read/write winding passes through all cores in a vertical row for all 16 or 18 mats. Through the use of selection circuits, which control the current applied to specific X-Y windings, any one of the 32,768 word locations can be addressed for writing data into memory or reading data out of memory. Each mat has unique lines threading all of its cores to provide the sense/inhibit functions. There are two sense/inhibit lines per mat. The sense/inhibit lines as well as the selection circuits, are discussed in subsequent paragraphs.

3.3 MEMORY OPERATION

Figure 3-1 illustrates a typical portion of the core memory. X and Y wires pass through each core in the mat. The current passing through any one winding is such that no single winding produces a magnetic field strong enough to cause a core to change its magnetic state. Only the reinforcing magnetic field caused by the coincident current of both an X and a Y winding can cause the core located at the point of intersection to change states. It is this principle that allows the relatively simple wiring arrangement to select one and only one memory core out of the possible 32,768 contained on each mat. The current passing through either an X or Y winding is referred to as a half-select current.

A half-select current passing through the X3 winding (Figure 3-1) from left to right produces a magnetic field that tends to change all cores in that horizontal row from the 1 to 0 state. The flux produced by the current is, however, insufficient to cause the state transition in any core. Simultaneously passing a half-select current through the Y2 winding from top to bottom produces the same effect on all cores in that particular vertical row.

Note, however, that both currents pass through only one core, which is located at the intersection of the X3 and Y2 windings. This is the selected core and the combined current values are sufficient to change the state of the core. The arrows in Figure 3-1 show X and Y current direction for the read operation.



11-1790

Figure 3-1 Three-Wire Memory Configuration

All X and Y windings are arranged in such a manner that whenever a half-select current is passed through one line of each set, the resultant magnetic fields combine in the core at the point of intersection. This combined, full-select current ensures that the selected core is left in the binary state after a read operation, and in a binary 1 state after a write operation. The currents used to select the core are referred to as read or write currents. A typical hysteresis loop for a core is shown in Figure 3-2. The loop is always traversed in the direction of the arrows.

HYSTERESIS LOOP FOR CORE

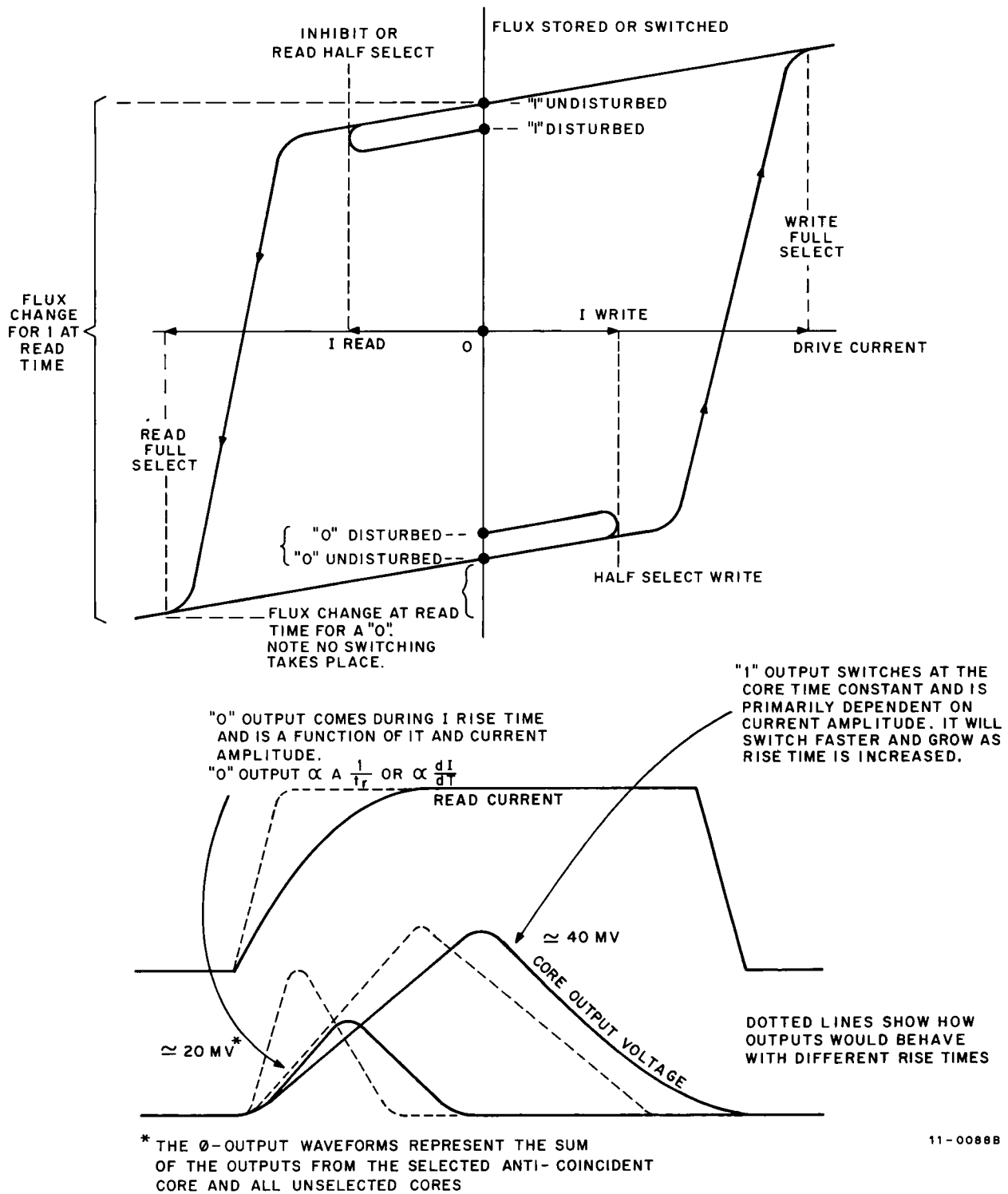


Figure 3-2 Hysteresis Loop for Core

In the MF11-W/WP Core Memory, every X winding serially threads 128 cores of each of the 16 or 18 mats; every Y winding threads 256 cores of every mat. Therefore, whenever a full-select current flows through a selected core on one mat, it also flows through an identical core on all of the other 15 mats. The X3-Y2 cores on all mats switch together, causing each of the 16 cores to become one bit of a 16-bit word.

Because of the serial nature of the X-Y windings, a method must be employed to set certain cores to the 0 state; otherwise, every 16-bit word selected would be all 1s. The method used in the MF11-W/WP Core Memory is to first clear all cores to the 0 state by reading. During the write operation, cores on particular mats are inhibited by an inhibit winding. The inhibited cores remain 0s even when identical cores on other mats are set to 1s.

The half-select current for the inhibit lines is applied from an inhibit current driver, which is a switch and a current source between the inhibit line and +20 V. The current in the inhibit line flows in the opposite direction from the write current in all Y lines and cancels out the write current in any Y line. There are separate inhibit drivers for each memory mat, and each mat represents one bit position of a word; thus, selected bits can be inhibited to produce any combination of binary 1s and 0s desired in the 16-bit word. Remember that the inhibit function is active only during write time.

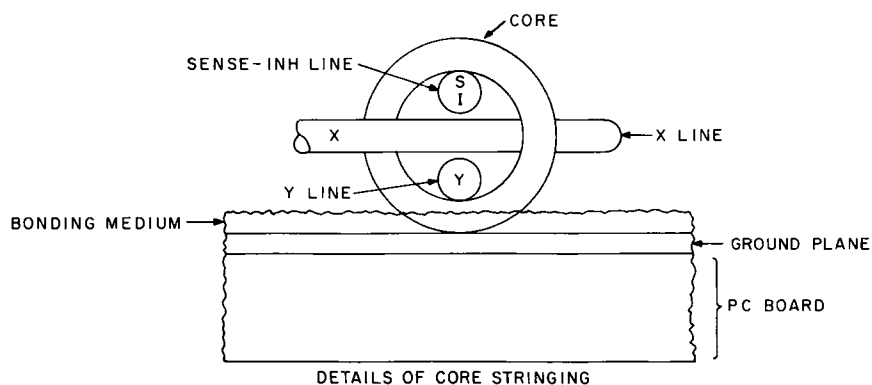
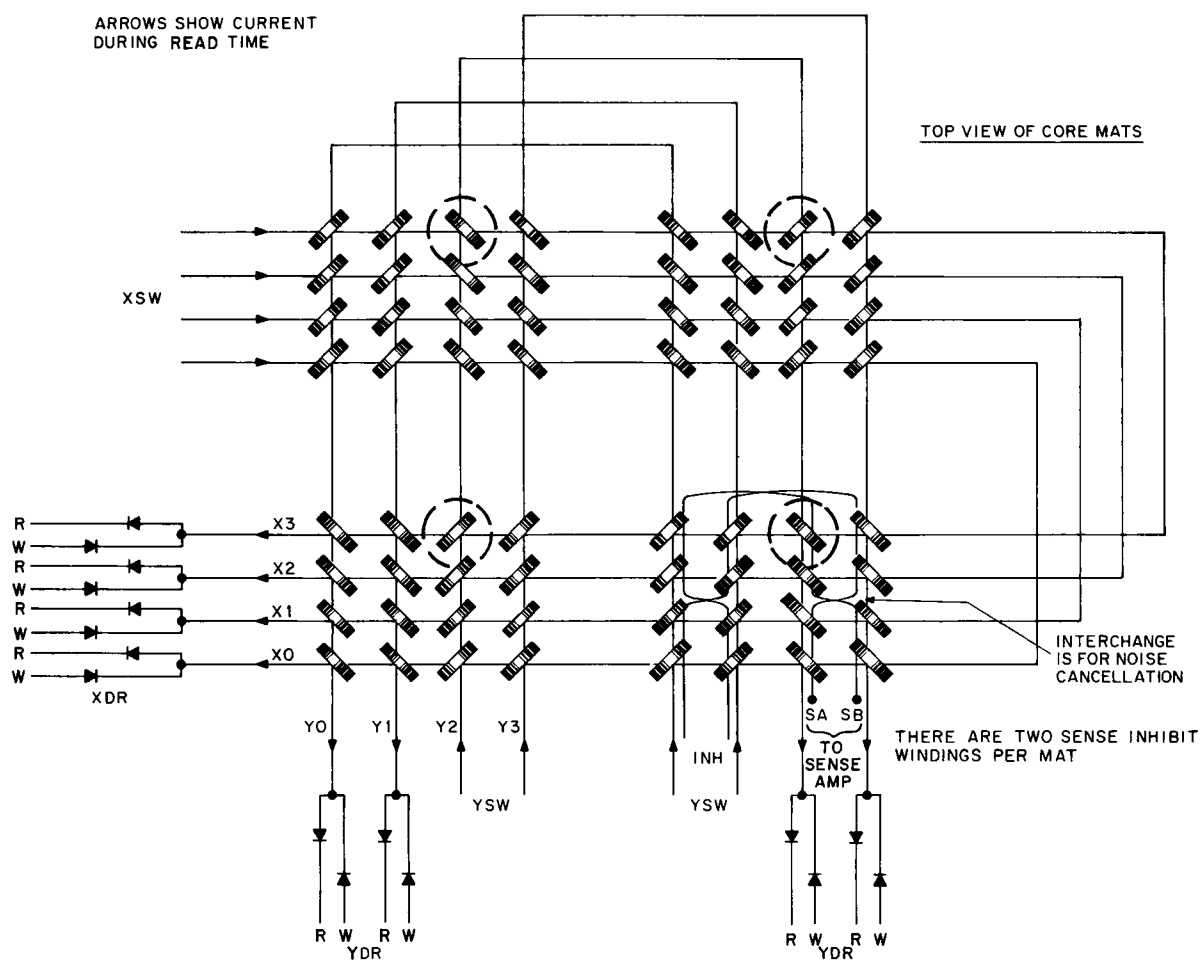
The sense/inhibit lines are also used to read out information in a selected 16-bit memory cell. The specific core is selected at read time in the same manner as during the write cycle, with one notable exception: the X and Y currents are in the opposite direction than they are for the write operation. These opposite half-select currents cause all cores previously set to 1 to change to 0; cores previously set to 0 are not affected. Whenever the core changes from 1 to 0, the flux change induces a voltage in the sense winding of that mat. This voltage is detected and amplified by a sense amplifier. The amplifier output is strobed into the data register for eventual transfer to the Unibus.

Figure 3-3 shows a 16-word by 4-bit planar memory. The MF11-W/WP Core Memory functions in the same manner, except that it has 256 X lines, 128 Y lines, and 16 core mats. The core stringing is identical, and the sense windings are strung through two groups of 16,384 cores with the interchange between X127 and X128, instead of between X1 and X2.

3.4 X AND Y DECODING

The basic decoding units are type 7442 and 74154 4-line to 10-line, and 4-line to 16-line decoders. The inputs are D0, D1, D2, and D3; they are weighted 1, 2, 4, and 8, with D0 being the least significant bit. An output is selected according to the sum of the weighted inputs. The selected output is low and all others are high. See Appendix A for truth tables of 7442 and 74154 decoders. Each 7442 controls eight read/write driver pairs and each 74154 controls sixteen read/write switch pairs. This switch matrix is combined with the stack X-Y diode matrix to allow selection of any location out of the total 32,768 locations (see stack drawing D-CS-5411644-0-1) for interconnections).

The X and Y line switches are first differentiated as switches and drivers. The drivers are those switches that are connected to the diode end of the stack. Drivers and switches are further differentiated by function: either read or write. Another differentiation is made by polarity: negative or positive, depending on the physical connection. Read switches and write drivers are connected to the current generator outputs and are considered positive; write switches and read drivers are connected to ground and are considered negative.



11-3807

Four mats shown for a 16-Word by 4-Bit Memory

Figure 3-3 Three-Wire 3D Memory

3.5 DRIVERS AND SWITCHES

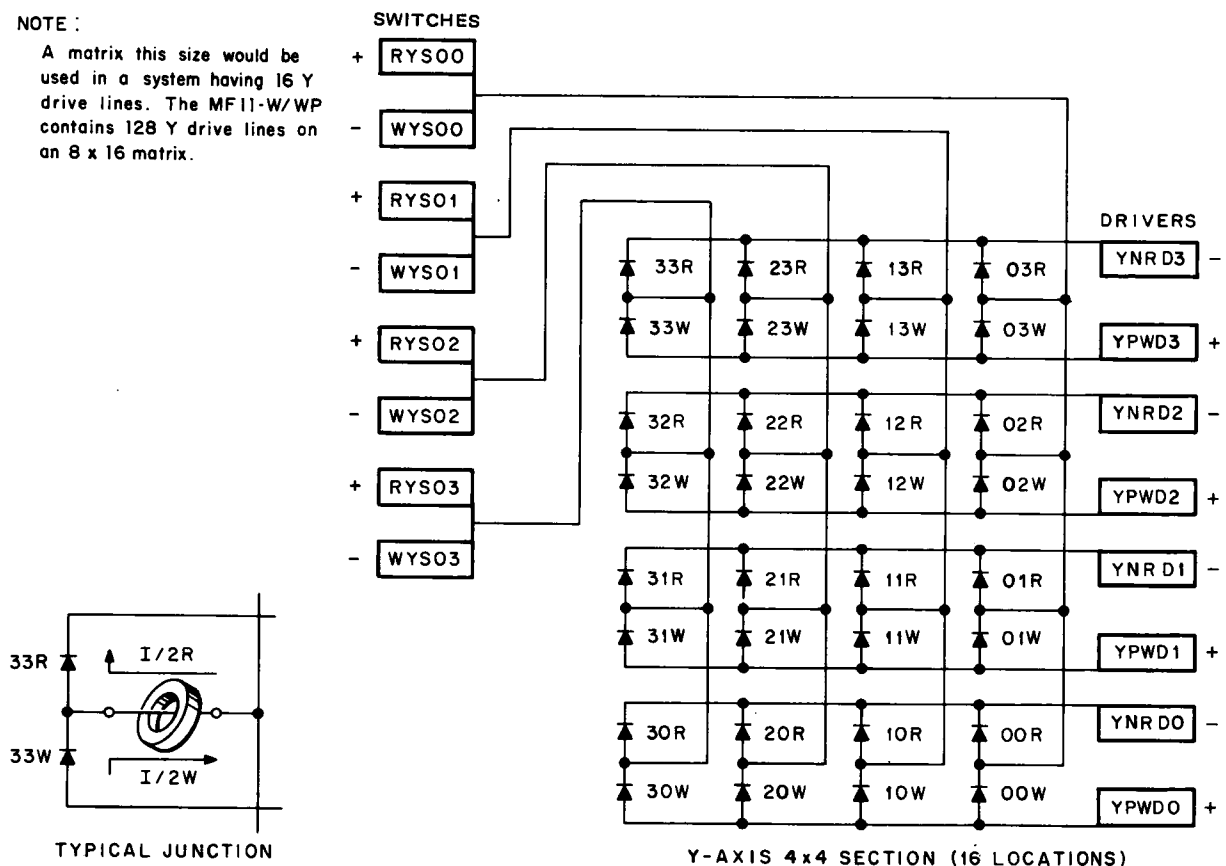
Drivers and switches direct the current through the X and Y lines in the proper direction as selected by the read and write operations. Each switch or driver is addressed by one decoder output. A low decoder output selects the associated read and write switch or driver.

In the MF11-W/WP Memory, 16 pairs of read/write switches and 16 pairs of read/write drivers are provided in the X axis; 16 pairs of read/write switches and 8 pairs of read/write drivers are provided in the Y axis. In conjunction with the stack diode matrix (drawing 5411644-0-1), this allows selection of 256 lines in the X axis and 128 lines in the Y axis. This provides a 256×128 matrix that selects any location out of 32,768 locations.

Figure 3-4 illustrates a portion of a Y selection matrix and shows the interconnection of the diodes and the lines from the switches and drivers. It shows how 4 pairs of switches and drivers are connected to select one of 16 lines. Refer to drawing 5411644-0-1, for an extension of this method which uses 16 pairs of switches and 8 pairs of drivers to select one of 128 lines.

NOTE :

A matrix this size would be used in a system having 16 Y drive lines. The MF11-W/WP contains 128 Y drive lines on an 8×16 matrix.



11-3922

Figure 3-4 Simplified Y Line Selection
Stack Diode Matrix

To illustrate the operation of the actual X matrix or Y matrix, a smaller, but analogous, Y matrix is shown in Figure 3-4. This matrix shows four pairs of drivers and four pairs of switches for a Y axis (16 Y drive lines).

Polarities are shown for convenience. The diodes are identified to assist in associating them with the drivers and switches. Each line from a twin diode interconnection to a read/write switch pair passes through 128 cores and represents one line on each bit mat. Assume that a read operation is to be performed and the word address decoders have selected read switch RYS00 and read YNRD1. The Y current generator sends current through read switch RYS00 (conventional flow) which puts a positive voltage on the anodes of diodes 03R, 02R, 01R, and 00R. The non-selected read drivers (YNRD3, YNRD2, and YNRD0) provide a positive voltage on the cathodes of their associated diodes (03R, 02R, and 00R, respectively) which reverse biases them and prevents conduction. Read driver YNRD1, which has been selected, turns on and makes the cathode of diode 01R negative with respect to the anode which forward biases it. The diode conducts and allows current to flow to write driver YNRD1. A half-select current now flows through this line that links 256 cores per bit mat (4096 total for 16 mats).

Figure 3-5 is a simplified schematic of two pairs of switches and drivers in the MF11-W/WP interconnected with the core stack and current generator. Read/write switches YS07 and read/write drivers YD7 are used as examples. These switches and drivers are chosen for convenience. For a read or write operation, there are 128 switch/driver combinations on the Y axis and 256 on the X axis. For a write operation, decoder E30 selects positive write driver E31 and decoder E16 selects negative write switch E19. Both E31 and E19 are turned on when they are selected and write timing occurs. E31 conducts, which allows current from the Y write current generator to flow through the associated matrix diode, and the cores on the selected line. After passing through the cores, the current flows through a transistor to ground. For a read operation, decoder E16 selects positive read switch E20 and decoder E30 selects negative read driver E32. Both E20 and E32 are turned on by read timing. E20 conducts, which allows current from the Y read current generator to flow through D47, and the cores in the opposite direction. After passing through the cores, the current flows through the associated matrix diode to ground. Read current flow is shown as a broken line; a solid line shows write current flow.

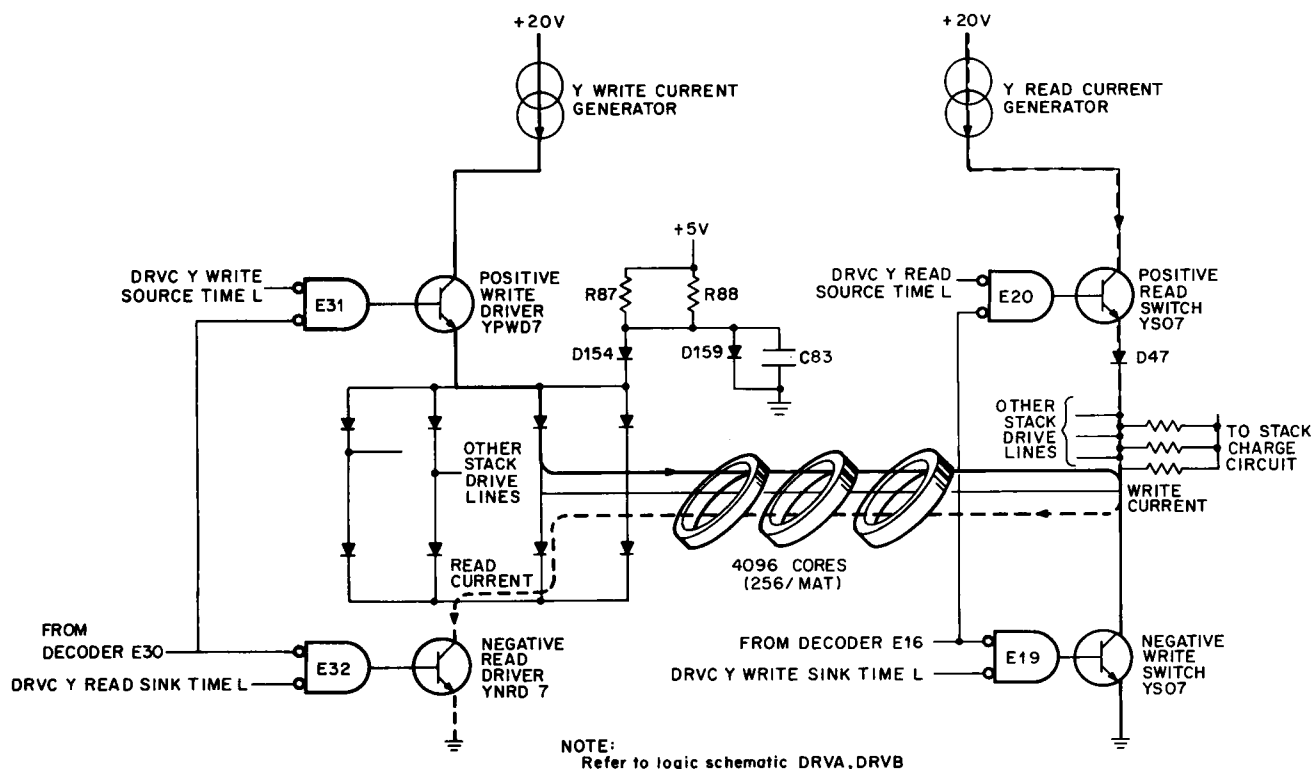


Figure 3-5 Typical Y Line Read/Write Switches and Drivers

3.5.1 Word Address Decoding and Selection Sequence

This paragraph takes a specific word address through the decoding and X and Y line selection sequence. The word address is 017772 and it is assumed that a specific memory bank has been selected. The binary equivalent of the address is shown below. A read operation is to be performed.

ADDRESS BITS A<17:00>																		BIT POSITION
17	16	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	BINARY
0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	0	
0			1			7			7			7			2			OCTAL

11-1173

Bits A(15:01) are used to decode the word address. Bits A(15:01) are sent from the Unibus receivers to inputs to the associated word latches. Table 3-1 shows the state of bits A(15:01) and the decoding signals generated by the word address latches.

The decoders, switches, and drivers are shown in drawing G236-0-1, sheets 1, 2, and 3. Using the decoding signals in Table 3-1 and the operating characteristics of the decoders, it is possible to determine which decoder outputs have been selected for word address 017772.

Decoder E30 - D2 is high, D1 is low, D0 is high; selects output 5 (pin 6) which is read driver YNRD5.

Decoder E16 - D3 is low, D2 is high, D1 is high, D0 is high; selects output 7 (pin 8) which is read switch YS07.

Decoder E39 - D2 is high, D1 is high, D0 is high; selects output 7 (pin 9) which is read driver XNRD07.

Decoder E25 - D3 is low, D2 is high, D1 is low, D0 is high; selects output 7 (pin 8) which is read switch XS07.

Table 3-1 Example of Word Address Decoding Signals

Address Bit	Unibus Receiver Input	Receiver Output	Latch State	Latch Output Signals
A01	L	H	set	A01H=H
A02	H	L	reset	A02H=L
A03	L	H	set	A03H=H
A04	L	H	set	A04H=H
A05	L	H	set	A05H=H
A06	L	H	set	A06H=H
A07	L	H	set	A07H=H
A08	L	H	set	A08H=H
A09	L	H	set	A09H=H
A10	L	H	set	A10H=H
A11	L	H	set	A11H=H
A12	L	H	set	A12H=H
A13	H	L	reset	A13H=L
A14	H	L	reset	A14H=L
A15	H	L	reset	A15H=L

3.6 READ/WRITE CURRENT GENERATION AND SENSING

Aside from the addressing and control logic, four functional units are involved in generating current to switch the cores and detect their state. The X and Y line read and write current generators supply the drive current (via switches and drivers); the inhibit drivers allow 0s to be written during a write operation; the sense amplifiers detect 1s during a read operation; and the Memory Data Register (MDR) temporarily stores data to be written or data that has been read from the memory. The following paragraphs discuss each functional unit and their interrelation.

The discussion of the read/write operations shows the interrelation of the current generator, inhibit drivers, sense amplifiers, and memory data register. Details of the operation of each functional unit are discussed in subsequent paragraphs. Several control signals are mentioned; however, details of their generation and timing are described in Chapter 2.

UNIBUS

8641 E51

SINA OUTPUT EN L

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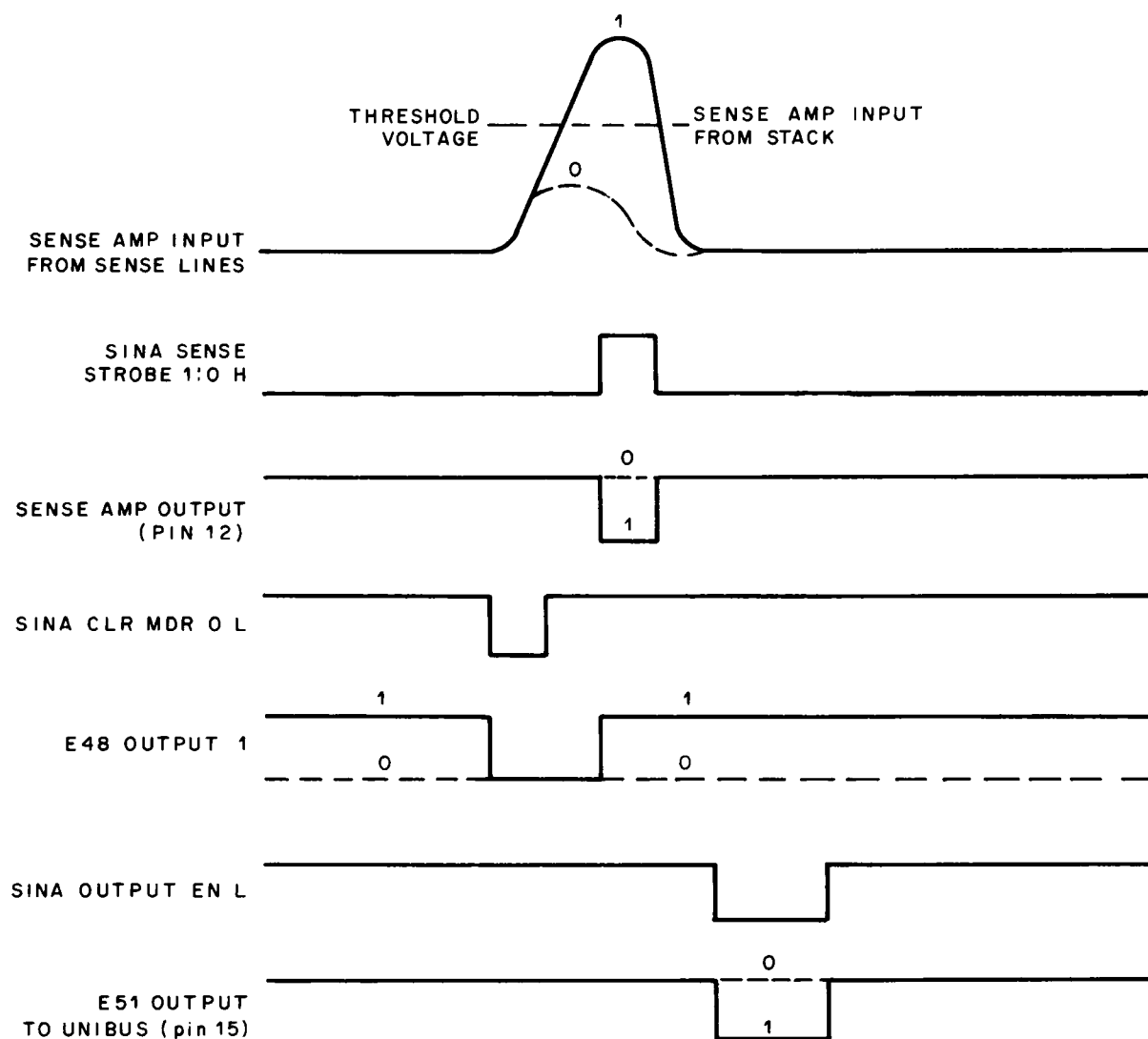
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3-9

During a read operation, half-select currents flow in one X and one Y line in each bit mat to select a word. These currents flow opposite to the write currents; therefore, cores in the 1 state are switched to the 0 state and cores in the 0 state are unchanged. Switching the core from the 1 state to the 0 state induces a voltage pulse in the sense winding. This pulse is detected by sense amplifier E50 as a differential voltage on input pins 6 and 7 if it exceeds the threshold reference voltage. This pulse is amplified and when SINA SENSE STROBE 0 H is generated at pin 15, the output of sense amplifier E50 goes high. Just prior to the strobe signal, the control logic generates SINA CLR MDR 0 L which clears (resets) flip-flop E48. The sense amplifier output is sent to the preset input (pin 10) of MDR flip-flop E48. A low on the preset input sets the flip-flop; its 1 output (pin 9) is a high. The high from pin 9 of the flip-flop is sent to input pin 14 of Unibus transceiver E51. The other input to E51 is SINA OUTPUT EN L. When the control logic generates SINA OUTPUT EN L, the output of E51 (pin 15) is low (logical 1 for Unibus logic). This is the readout of bit D07 and is sent to the requesting device via the Unibus. Timing diagrams for the sense operation are shown in Figure 3-7.



NOTE :

Refer to figure 3-6 for typical circuit schematic.

11-3833

Figure 3-7 Sense Operation Timing Diagram (Bit D07)

The read operation is destructive; all cores at the specified location are now 0. The data that was read must be restored by a write operation which immediately follows the read operation. Flip-flop E48 is still in the set state. The control logic generates the inhibit driver control signal SINA INH 1 L or SINA INH 2 L which is sent to the input of gate E46 (pin 3 or 12). The selected gate is not turned on and the respective inhibit driver is not turned on. With no inhibit current in the inhibit line to oppose the half-select Y line current, a 1 is written back into the appropriate cores.

In this example, if bit D07 is a 0 in core, it does not switch during the read operation and the output of sense amplifier E50 does not go high. Flip-flop E48 remains cleared (reset); its 1 output (pin 9) is low. When the control logic generates SINA OUTPUT EN L, the output of Unibus transceiver (pin 15) is high (logical 0 for Unibus logic). During the subsequent write operation, SINA INH 1 L, or SINA INH 2 L, is generated. This activates the respective inhibit driver which produces a current that opposes the Y line current and prevents a 1 from being written into this bit of the selected word.

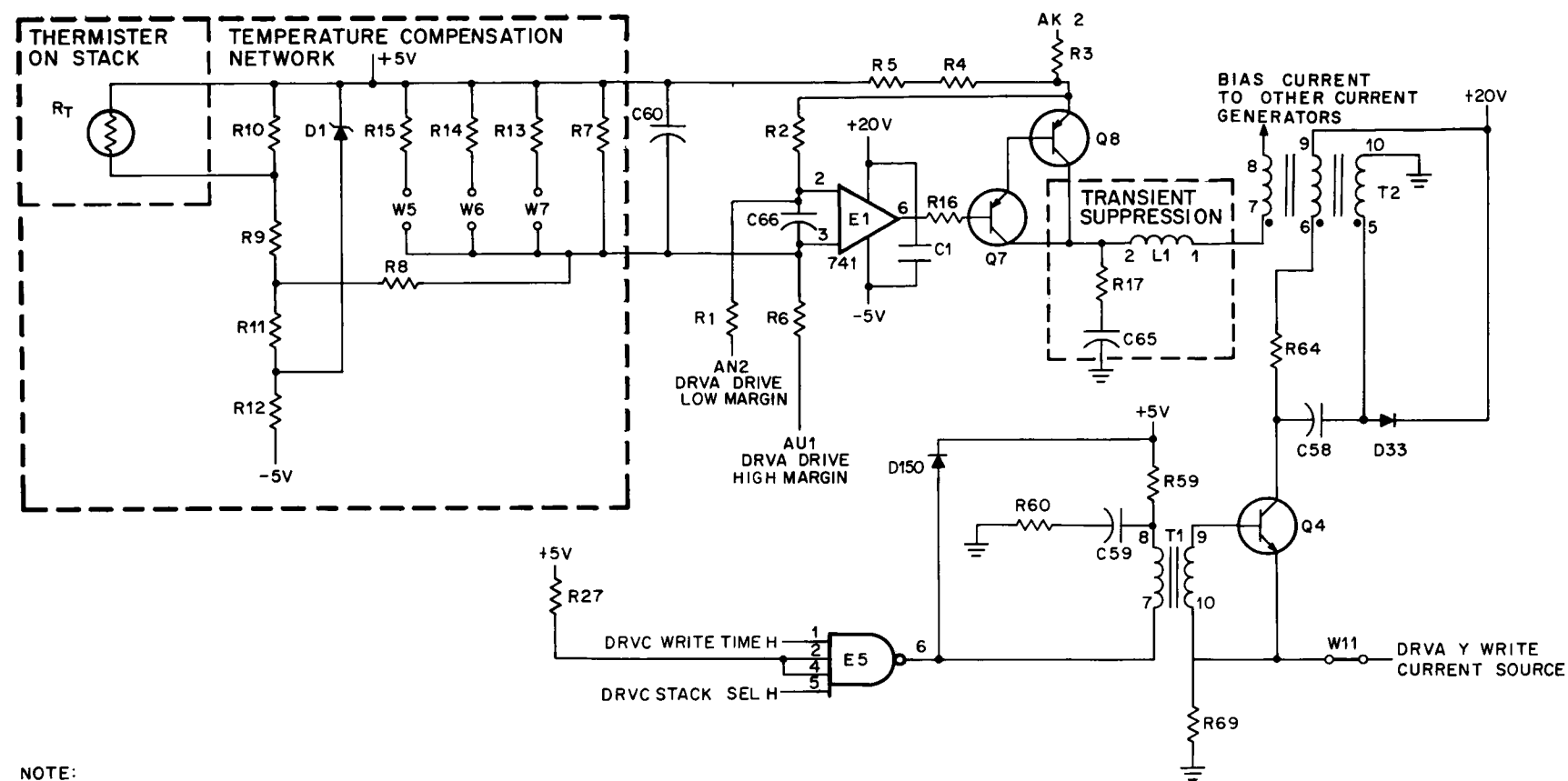
The read/write operation which has been discussed is a read/restore operation (DATI). The requesting device wants to read a word from memory and, as an internal requirement, the memory must restore the word by writing it back in core. In this case, the MDR flip-flops are preset by the sense amplifier outputs when 1s are read from the core. The flip-flop outputs are used in the subsequent write (restore) operation to control the inhibit drivers. If the requesting device wants to write a word into memory (DATO), it must load the data into the MDR flip-flops. The device asserts the data onto the Unibus from which it is picked off via Unibus transceivers. In this example, bit D07 is sent to pin 15 of Unibus transceiver E51. The bit is inverted by the transceiver and sent to the D input (pin 12) of flip-flop E48. At the start of the DATO cycle, the control logic generates SINA CLK MDR 0 H which clocks the flip-flop. If the D input is high, E48 is set. The selected inhibit driver is turned on by SINA INH 1 L or SINA INH 2 L. A 1 is written into the selected core. If the D input is low, E48 is reset. SINA INH 1 L or SINA INH 2 L is generated and the respective inhibit driver is turned on. A 0 is written into the selected core. Because SINA CLR 0 L, SINA SENSE STROBE 0 H and SINA SENSE STROBE 1 H are disabled in this mode, the read operation is used only to magnetically clear the cores.

3.6.3 X and Y Current Generators

A read and write current generator is provided for both the X and Y drive lines. The current generators and associated bias current supply are shown in drawing G236-0-1, sheet 4.

Optimum core switching requires current pulses of precise amplitude, duration, and shape. The current amplitude is controlled by the dc bias current supply (which is temperature-compensated). Pulse shaping is achieved by resistor, diode, zener diode, anti-overshoot circuits; duration is controlled by the timing pulses from the delay lines.

Figure 3-8 shows the bias current supply and write Y current generator. The heart of the current generators on both the G236 (X-Y current generators) and the G116 (inhibit current generators) modules are special saturating transformers. T2 is the saturating transformer for the write Y current generator. T2 is normally saturated very hard by bias current in the winding designated with pins 7 and 8. In order for the magnetic core of T2 to start to switch its magnetic flux in the opposite direction, the ampere turns applied by the bias current needs to be exceeded by an equal but opposite current in another winding. As long as T2 remains saturated, it is a low impedance to changes in current in any of its windings; however, once T2 starts to switch magnetic flux, large voltages may be induced across its windings in response to any additional changes in net current. That is, T2 acts like an ideal current source - low impedance with less than a specified current in winding 6-9 and a high impedance to additional current changes once the specified current amplitude is reached. This specified current is primarily determined by the bias current amplitude and the turns ratio of T2. The third winding of T2 (5-10) conducts current only after the drive current pulse has ended, and restores some current to the +20 V supply during that period. Although some losses occur in T2, most of the energy absorbed by T2 during the current pulse is restored to the power supply at the end of the pulse.



11-3805

Figure 3-8 Bias Current Supply and
Write Y Current Generator

The bias current supply provides the dc bias current required for all the saturating transformers on the G236 and G116 modules (in series). An LRC filter network is provided to ensure that the bias current does not acquire ac components and to ensure that large voltages do not build up along the series path. (L1, C65, and R17 comprise such a filter network protecting Q7 and Q8 from transients.) The resistor network consisting of the stack thermistor, R10, R11, R12, R8, R7, R13, R14, R15, and zener diode D1, provides a temperature compensated reference voltage to pin 3 of E1. R2 feeds back the emitter voltage of Q8 to pin 2 of E1. The 741 operational amplifier uses its gain to adjust its output (pin 6) so that the voltage on pin 2 is made very nearly equal to the voltage on pin 3. In this way, the amplifier circuit causes a current to flow through R4 and R5 controlled precisely by the reference voltage on pin 3 of E1. By measuring the voltage on AK2 with respect to +5 V, a very accurate measure of the bias current can be made, since most of the current through R4 and R5 finds its way through the collectors of Q7 and Q8 (Q7 base current is small) and becomes the bias current.

NOTE

The memory protection circuits and the circuitry to detect loss of bias current are described in Chapter 2.

Module pins AN2 and AU1 provide a means of changing the amplitude of the bias current. Grounding AU1 through a 470K ohm resistor (R6) will cause the bias current to be reduced, and grounding AN2 through a 470K ohm resistor (R1) will increase the bias current. This capability becomes important for margining the memory.

CAUTION

Jumpers W5, W6, W7 are factory-cut to adjust the bias current to its optimum value and they should not be changed.

In Figure 3-8, the operation of the write Y current generator is as follows. The output of E5 (pin 6) will go low when the current generator turns on. Current is coupled through T1 to saturate transistor Q4. At this point, current may flow through T2 windings (pins 9 and 6 and 5 and 10), through Q4 and to the write Y switches.

A diode and resistor network forms an anti-overshoot circuit in the write Y circuit which conducts current only during the rise time of the current. Its function is to "steal" some of the write X current during the rise time so that when the current overshoot occurs, the overshoot only serves to bring the current quickly up to its proper value (and not beyond it). It is connected at the write X current source output.

R64 and C58 primarily serve as a dc current limit and as a rise time aid, respectively.

When Q4 is turned off by E5 (coupling through T1) current will flow through D33 until the core of T2 has been completely resaturated by the bias current. This places energy back in the power supply.

3.6.4 Inhibit Driver

A detailed schematic of the inhibit driver for bit D07 is shown in Figure 3-9; it is typical of all 16 inhibit driver pairs (drawing G116-0-1).

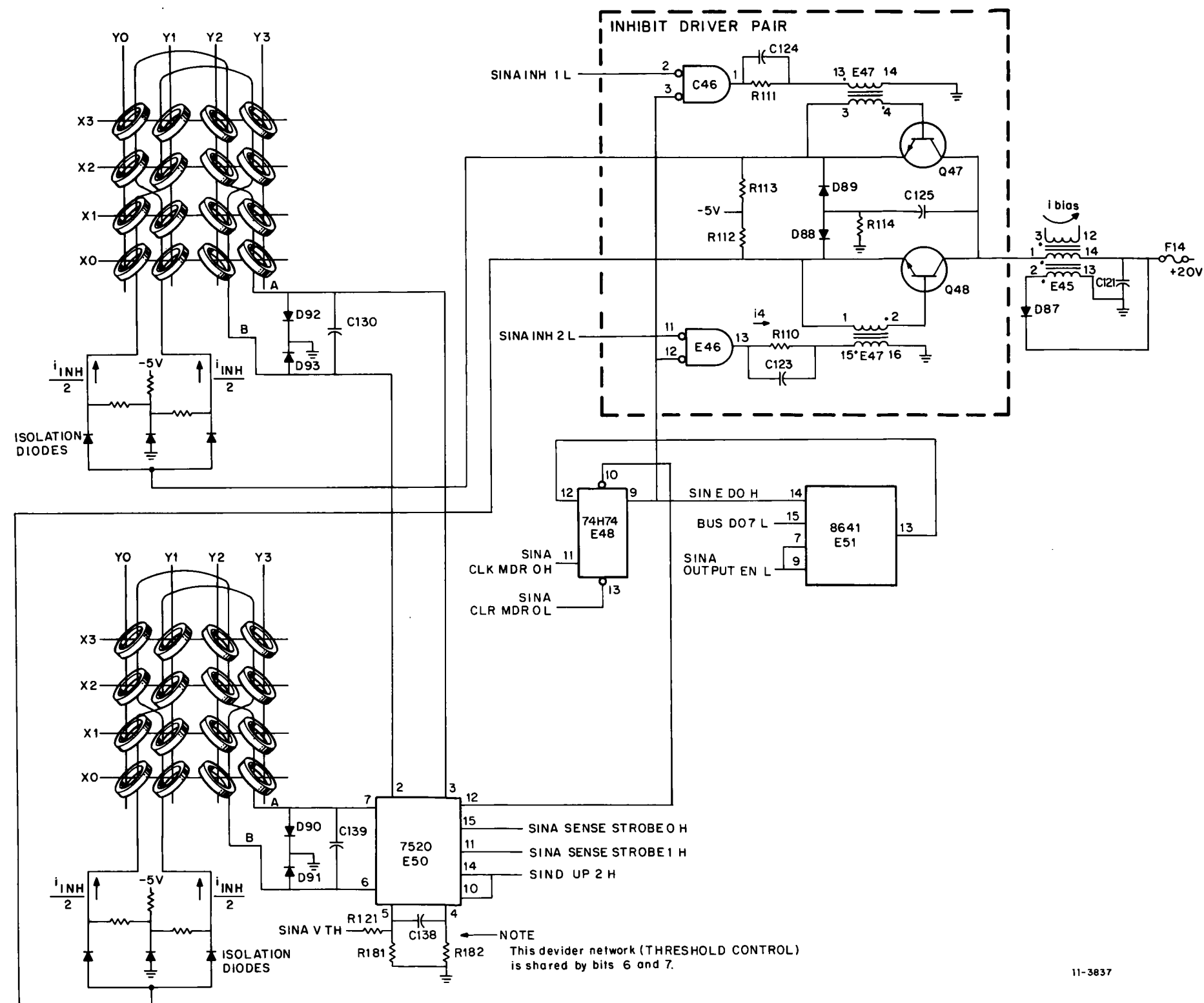


Figure 3-9 Sense Amplifier and Inhibit Driver

Address bits 02 controls the selection of the appropriate sense amplifier and inhibit driver to use with a selected address. When A02H is low, the selected Y drive line is between 0 and 63. When A02H is high, the selected Y drive line is between 64 and 127. Therefore, sense amplifier 0 and inhibit driver 0 are selected when A02H is low; and sense amplifier 1 and inhibit driver 1 are selected when A02H is asserted. To write a zero in bit seven of a selected word, the output of gate E46 (pin 1 or 13) goes high, driving current through the primary winding of E47 to which the selected gate is connected. The secondary winding of that transformer provides the current to turn on Q27 or Q28. When Q27 is turned on, current flows from the +20 V through fuse F14, saturating transformer E45, transistor Q27, isolation diodes, the sense/inhibit winding, and the isolation diodes D92 and D93 to ground. The value for the inhibit current is primarily determined by the bias current to E45 transformer (winding 3-12).

Each leg of the sense/inhibit sees half the inhibit current; approximately 370 mA. Capacitor C125, diodes D88 and D89, and resistor R14 help reduce the power dissipated in Q27 and Q28 turn-off.

The respective inhibit driver is turned off when the output (pin 1 or 13) of gate E46 goes from high to low. At turn-off time, the back emf caused by the stack inductive reactance tries to drive the emitter of Q27 highly negative; however, diodes D88 and D89, and resistor R114 help to clamp this voltage to ground.

Capacitors C123 and C124 allow the gates to pump reverse current into the transformer primaries; they also help to decrease the turn-on time of Q27 and Q28.

3.6.5 Sense Amplifier

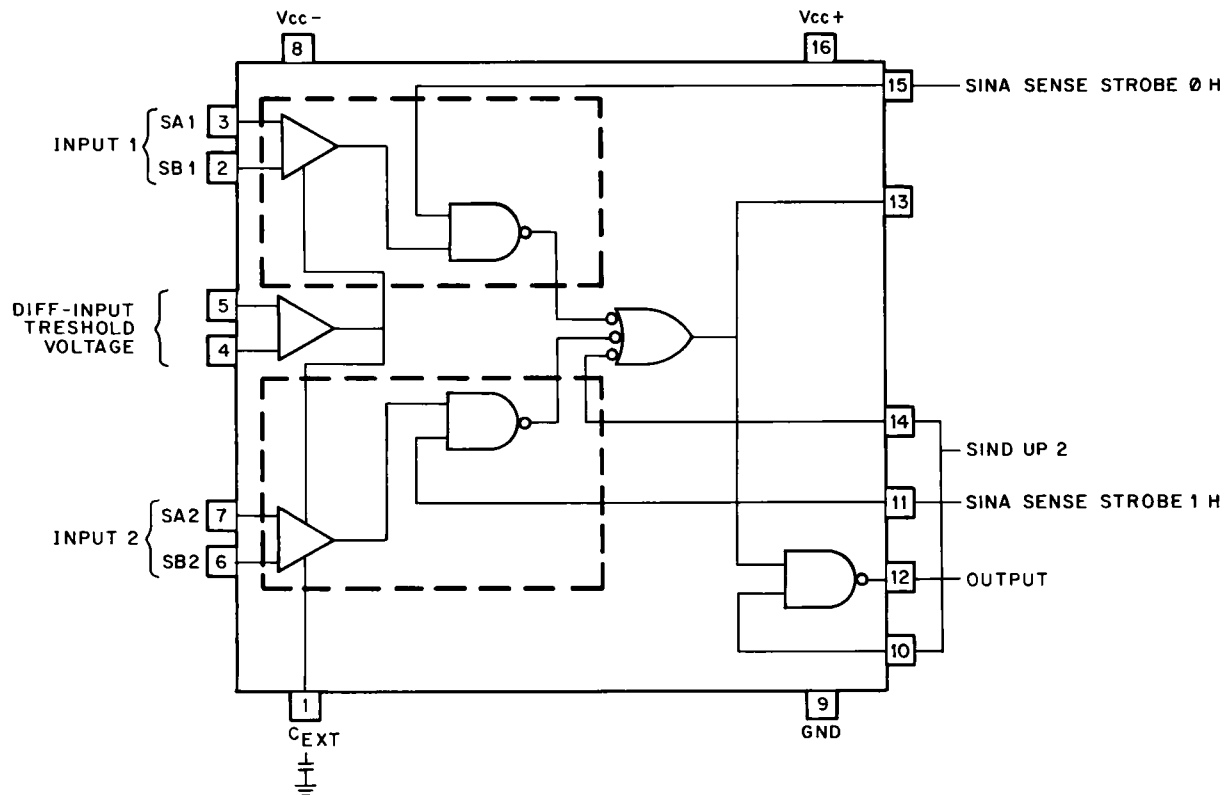
A detailed schematic of the sense amplifier circuit for bit D07 is shown in Figure 3-9; it is typical of all 16 sense amplifier circuits (drawing G116-0-1). It consists of the sense amplifier, terminating capacitor for the sense/inhibit winding, and threshold voltage network.

Each sense amplifier input connects to 16K cores. During a sense operation, the inhibit driver connection is an open circuit through driver transistor Q27 or Q28. The effect of the inhibit driver circuits, and isolation diodes D92 and D93 or D90 and D91 can be ignored during the sense operation because the diodes are reversed-biased.

Sense amplifier E50 (type 7520), being a dual IC package, connects to both S/I lines of one mat. A simplified block diagram of the package is shown in Figure 3-10. Each interior circuit consists of a preamplifier and sense amplifier. The inputs to the internal sense amplifiers are available to facilitate accurate strobe timing. Both circuits share a reference voltage (or threshold voltage) amplifier (pins 4 and 5). In this application, pin 4 is grounded through resistor R182 and a positive threshold voltage of approximately 17 mV is supplied to pin 5. This voltage is obtained from the +5 V supply via the resistor voltage divider (see Figure 3-9). Operation of the sense amplifier is discussed in Paragraph 3.6.2.

3.6.6 Memory Data Register

The Memory Data Register (MDR) is a 16-bit flip-flop register that is used to store a word after it is read out of the memory, or to store a word from the Unibus prior to its being written into the memory. It is composed of eight 74H74 dual high-speed D-type flip-flops. At the start of a memory read operation, the MDR is cleared directly via the CLEAR input (pin 1 or pin 13) of each flip-flop; the clear signal is SINA CLR MDR 0 L for bits D00-D07, D16, and D17 and SINA CLR MDR 1 L for bits D08-D15, D18, and D19. The operation of the MDR during a read/restore operation (DATI) and a write operation (DATO) is discussed in Paragraph 3.6.2.



11-3836

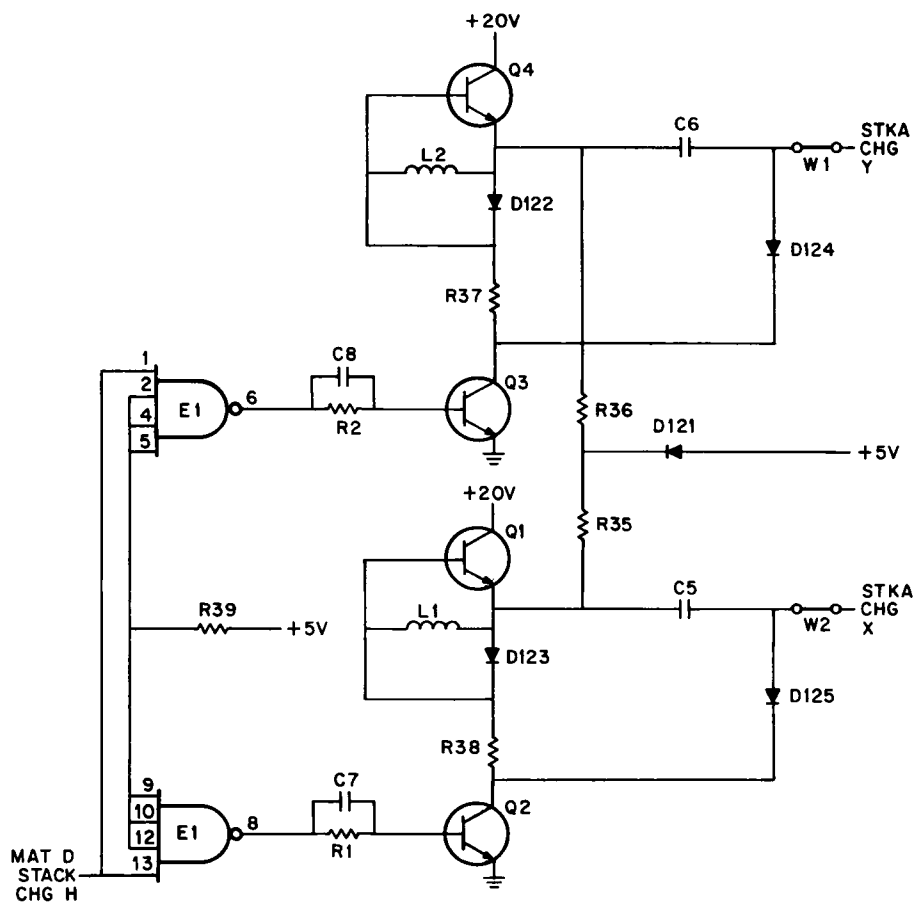
Figure 3-10 Type 7520 Dual Sense Amplifiers

3.7 STACK CHARGE CIRCUIT

The stack charge circuit assists the stack capacitance in recovering and shortens the rise time of the stack current. It also reduces unwanted currents in the seven unselected lines associated with the selected driver. It is located on the H224 module.

Figure 3-11 shows the stack charge circuit. The outputs are taken from the emitter of transistors and go to the junctions of each X and Y read/write switch pair via a capacitor and jumper. During a read operation, these outputs must be low (approximately 0 V). During a write operation, the outputs are approximately +12 V. The effective stack capacitance associated with each set of lines is shown as C_{STACK} .

During a read operation, the MATD STACK CHG H signal goes low, making the output of E1 (pin 6 and 8) high, thus saturating Q2 and Q3, and turning on Q1 and Q4. The output voltages of the circuit is also held low by the parallel combination of L1 and D123, and also L2 and D122. A current thus flows from +5 V, through R3 and R36, through L1 and L2, through R37 and R38 and through Q2 and Q3, to ground. Q1 and Q4 are off since their base-emitter junctions are not forward-biased.



11-3839

Figure 3-11 Stack Charge Circuit

During a write operation, the MATD STACK CHG H signal goes high, making the output of E1 (pin 6 and 8) go low, thus turning off Q2 and Q3. Current that was flowing through L1 and L2 is forced to continue to flow, but now must flow into the base of Q1 and Q4. Hence, with Q1 and Q4 turned on (saturated) and Q2 and Q3 off, the output is equal to 20 V less $V_{CE SAT}$ of Q1 or Q4. Current spiking from Q1 and Q4 on the transitions is prevented by D122 and D123. When Q2 and Q3 turn on again, Q1 and Q4 must be fully off before current can flow through D122 and D123. This is due to the fact that if D122 and D123 are forward-biased, the base-emitter junction of Q1 and Q4 are reversed-biased.



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CHAPTER 4

MF11-WP CORE MEMORY WITH PARITY

4.1 INTRODUCTION

This chapter contains a description of the theory and operation of the MF11-WP parity memory and the M7259 Parity Controller. Inasmuch as the MF11-WP is similar to the MF11-W Memory, which is described in the main body of this manual, only those areas of operation which are unique to the MF11-WP are covered in this chapter.

NOTE

An M7259 Parity Controller module must be Etch Rev D and CS Rev E or higher to be useable in the MF11-WP.

4.2 DESCRIPTION

The parity memory consists of an M8294 32K Unibus Timing module, a G236 Driver module, a G116 Sense Inhibit module, and an 18-bit H224- Stack module. In addition, an M7259 Parity Controller module is required. The M7259 Parity Controller performs all parity generating and checking functions and communicates with memory via an internal bus, shown in Figure 4-1. The signals on the internal bus are shown in Figure 4-2 and are described in Paragraph 4.6.2. The parity controller processes 32K or 64K of memory (two MF11-WPs). Bits 16 and 19 are the parity bits for the low byte and high byte, respectively. These bits are the property of the parity controller and are not accessible to the PA and PB lines on the Unibus. Bits 17 and 18 are not used in the MF11-W or the MF11-WP. The stack may or may not contain the cores and/or electronics for these bits even though they are shown on the circuit schematic.

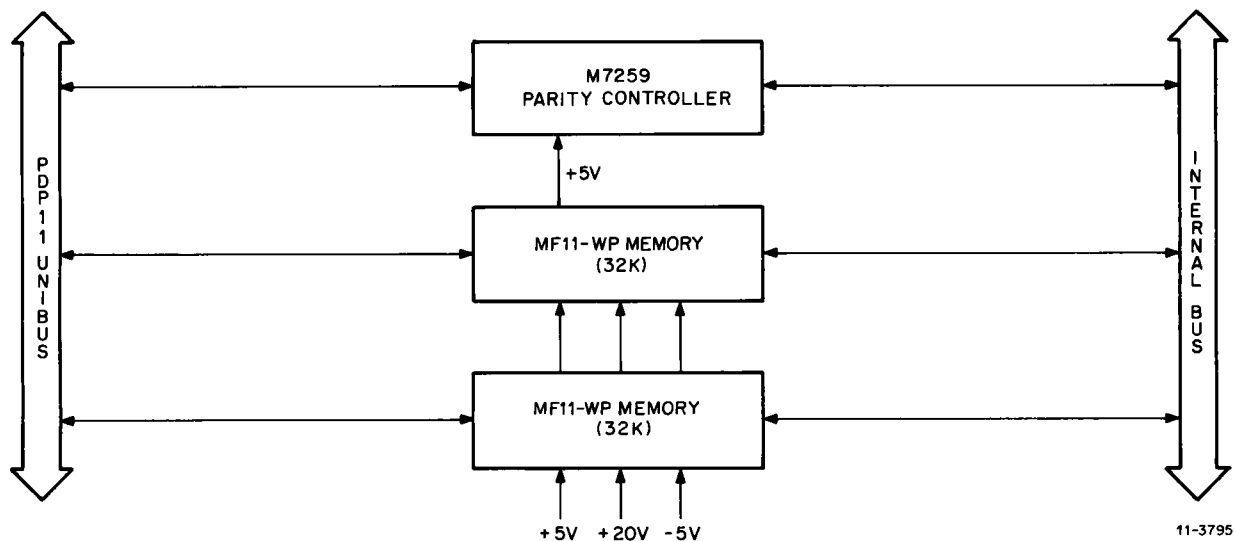


Figure 4-1 Parity Controller Internal Bus

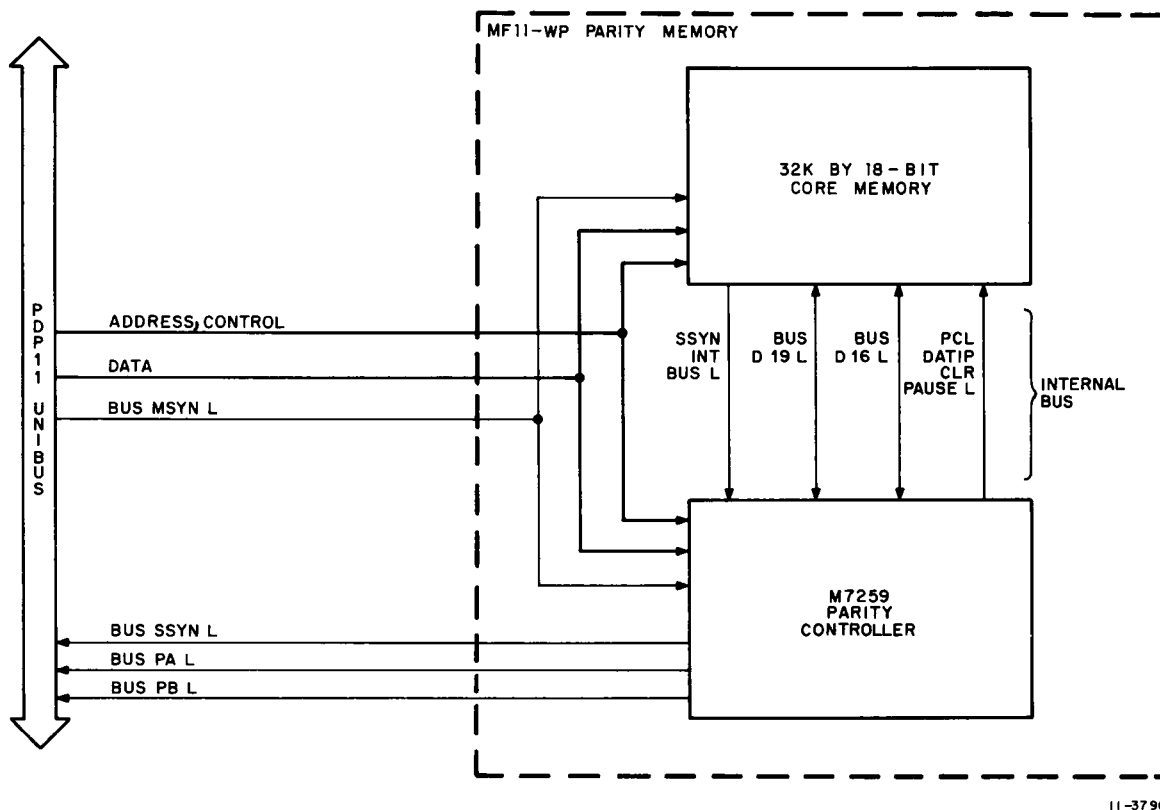


Figure 4-2 Parity Controller Block Diagram

In a DATO or DATOB bus cycle, both the low order and high order bytes are coded for odd parity; thus, for every byte containing an even number of 1s, a 1 is written into the corresponding parity bit location.

In a DATI or DATIP bus cycle, each byte plus its associated parity bit is checked for an odd number of 1s. If the sum is even, an error condition exists. When a parity error is detected during a DATIP, the erroneous data causing the parity error is saved and written back into core.

4.3 SPECIFICATIONS

The specifications of the M7259 Parity Controller are given in Table 4-1. Table 4-2 shows the cycle and access times for the MF11-WP Memory option.

4.4 FUNCTIONAL DESCRIPTION

The MF11-WP parity memory is read/write, random access, coincident current, magnetic core, parity memory with a maximum cycle time of 1150 ns and an access time of 525 ns maximum. It is organized in a 3D, 3-wire, planar configuration. Word length is 18 bits, two of which are the parity bits; the memory capacity is 32,768 (32K) words.

Table 4-1 M7259 Parity Controller Specifications

Voltage Requirements:	+5 V $\pm$ 5% with less than 0.05 V p-p ripple
Current Requirements:	1.2 A Maximum
Power Dissipation:	6 W Maximum
Environment:	
Ambient Temperature:	0° C to 60° C (32° F to 140° F)
Relative Humidity:	0–90% (non-condensing)
Unibus Unit Load:	1

Table 4-2 MF11-WP Maximum Cycle and Access Times

Bus Mode	Access Time	Cycle Time
DATI	500 ns	1150 ns
DATIP	500 ns	525 ns
DATO-DATOB (Pause Clear)	125 ns	1150 ns
DATO-DATOB (Pause Set)	100 ns	700 ns

The operation of the parity memory is identical to that of the MF11-W Memory, except for the parity generation and checking functions. In order to implement this option, an 18-bit stack module (H224-C) is used (bits 19 and 16 being the parity bits). In addition, a parity controller module is required. The controller is a dual height module (M7259) which plugs into the memory system backplane. It contains a Control and Status Register (CSR) and all the logic used to generate and check parity. A schematic diagram of the parity controller is shown on engineering drawing D-CS-M7259. Odd parity is used; if the number of 1s in a given byte is even, then a 1 will be written into the respective parity bit location. The use of odd parity allows detection of a memory failure of all 0s, which is a more probable failure mode than all 1s.

Error action can be disabled or enabled under program control. If parity error action is enabled by setting bit 0 of the CSR, a parity error will cause assertion of the parity error code on the Unibus. Processors equipped to detect Unibus memory parity errors will trap through vector 114 upon receipt of the parity error code. The error code is BUS PB L asserted and BUS PA L not asserted. (See Paragraph 4.5 in the programming section of this chapter.) On parity generation (DATO or DATOB) both the low order (D00 to D07) and the high order (D08 to D15) bytes are coded. The Unibus data is applied through buffers to the inputs of E4 and E13 on the M7259. The outputs of these ICs will be high if their respective inputs contain an odd number of 1s, and thus cause the D16 or D19 internal parity bits to be set. The D16 bit is the parity bit for the low order byte and the D19 bit is the parity bit for the high order byte. The BUS C1 L signal to the M7259 Parity Controller indicates whether parity is to be generated or checked.

4.4.1 DATI or DATIP Cycle

For parity checking (DATI or DATIP), the same two ICs which were used for parity generation are used; in this case, however, a low input indicates a parity error. During the memory read cycle, the signal SSYN INT BUS L is sent to the parity controller to indicate that memory data is present on the Unibus. This signal initiates a timing sequence (PCL SSYN DLY L) to allow for worst case propagation delays of data through the memory data drivers, parity controller data receivers, and the parity tree and checking logic. At the end of this sequence, one of two data input pulses to the parity error flip-flop occur; PC2 PARITY ERROR H or $\sim$ PC2 PARITY ERROR H. If each byte and its respective parity bit contain an odd number of 1s, then $\sim$ PC2 PARITY ERROR H is generated, allowing BUS SSYN to be sent to the bus master to indicate that data is available and valid. If, however, the sum of 1s of either byte is even, then the signal PC2 PARITY ERROR H is generated, causing CSR 15 to set (parity error indication). If parity error action is enabled (CSR0 = 1), then BUS SSYN and BUS PB signals will be enabled. The BUS PB signal indicates to the bus master that a parity error has occurred during the current DATI or DATIP cycle.

Since the restore portion of the memory cycle is skipped during a DATIP operation, provision must be made to save bad data in core in the event of a parity error during DATIP. The operation of the parity controller checking and timing sequence is the same as during a DATI operation, except that if PC2 PARITY ER DLY (0) H is generated, it will cause an 500 ns pulse, DATIP CLR PAUSE (1) L, to be generated. This signal causes the memory to restore the bad data, and also eliminates the requirement for the write cycle which would otherwise have to follow.

4.4.2 DATO Cycle

During a normal DATO cycle, that is, a DATO which does not follow a DATIP, parity is being generated before the read portion of the memory cycle. The Unibus data, along with the proper parity bits, are transferred into a data register on the G116 Sense Inhibit module. SSYN is then returned to the bus master via the parity controller to indicate that data has been strobed from the bus. Data is transferred from the data register to core during the write cycle.

If the DATO follows a DATIP, the sequence is altered. During the DATIP, the memory location will have been cleared and a PAUSE flag set. When the DATO occurs, the read cycle will be skipped, and the write cycle begun immediately. The data and parity bits are transferred from their respective buses at the beginning of the write cycle, at which time SSYN is generated.

4.4.3 DATOB Cycle

The DATOB cycle is similar to the DATO, except that during the DATOB, data is written in byte form rather than as a full word. The non-selected byte is simply restored along with the new data in the selected byte plus the parity bits.

4.4.4 Jumper Terminals

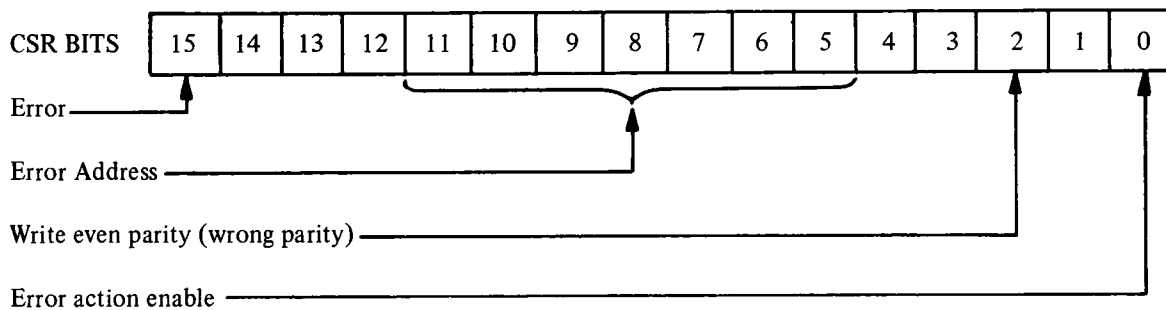
The M7259 Parity Control module contains seven sets of jumper terminals. The physical location of these terminals is shown in Figure 5-14 and the functions of the jumper terminals are listed in Table 4-3.

Table 4-3 M7259 Jumper Terminals

Jumper Terminals	Function
W1–W4	Discrete CSR address
W5	Modifies the timing constant for the SSYN delay one shot multivibrator (always out).
W6	When in, data is restored when a parity error is detected on a DATIP (always in).
W7	When out, SSYN is inhibited and the bus hangs when in the Maintenance Mode (always in).

4.5 PROGRAMMING

The Control and Status Register (CSR) is located on the M7259 Parity Controller. There is one CSR per 64K of memory. Transfer of a 16-bit control word from the processor to the CSR establishes the operating conditions of the MF11-WP. The data format of the CSR is shown below:



- NOTES:
1. All bits are read/write.
 2. All bits except the error address bits are cleared by INIT.

Bit	Name	Description
15	ERROR	Set when a parity error occurs regardless of whether any other response is enabled. Setting this bit will not cause a parity error trap. This bit is a flag and is not associated with the trap routine.
11:5	ERROR ADDRESS	Contains the highest order address bits of the most recent location causing a parity error.
2	WRITE EVEN PARITY (wrong parity)	Causes the controller to generate incorrect parity on write cycles (DATO or DATOB), forcing a parity error on the next DATI or DATIP cycle. This bit is intended for use as a diagnostic aid.
0	ERROR ACTION ENABLE	Enables error indication to the bus master when set.

The address of the CSR is hardwired in the range 772100 to 772136. Normally, the address 772100 is factory wired for the first 64K increment, 772100 for the second 64K, etc.

4.6 BUS LOADING

An MF11-WP represents two bus loads; one for the MF11-WP 32K Parity Memory module set and one for the M7259 Parity Controller. The M7259 Parity Controller handles the parity for 64K of memory. A second MM11-WP 32K module set adds one bus load. Therefore, the MF11-WP, expanded to 64K, would represent three bus loads.

4.7 INTERNAL BUS

The internal bus (Figures 4-1 and 4-2) is the communication path between the M7259 Parity Controller and the core memory. It comprises the following signals:

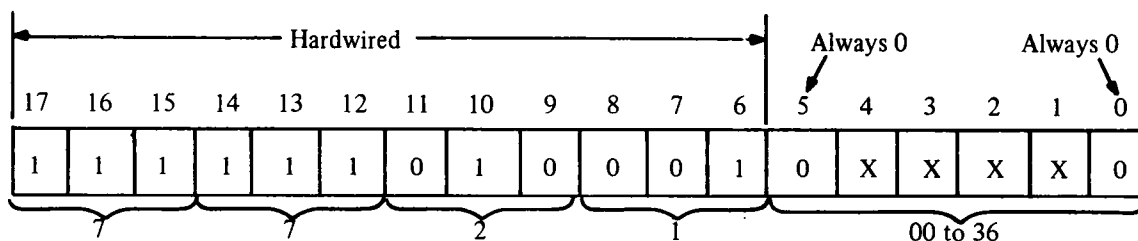
Name	Function
SSYN INT BUS L	Signals the parity controller when data is available on the Unibus to begin parity checking sequence.
PB INT BUS L (D19)	A bidirectional path which carries the generated parity bit to memory on DATO cycles and from memory to the controller on DATI cycles. This is the parity bit for the high order byte (D15:D08).
PA INT BUS L (D16)	Same as PB INT BUS L except that it is the parity bit for the low order byte (D07:D00).
DATIP CLR PAUSE (1) L	Clears the PAUSE flip-flop in the M8294 32K Unibus Timing module if a parity error occurs on a DATIP cycle, which initiates the write-restore cycle.
DATIP CLR PAUSE L	Not used with the MF11-WP.

4.8 INTERLEAVING RULES FOR PARITY MEMORY

1. Both of the memories to be interleaved must be parity memories.
2. The two parity memories to be interleaved must cover contiguous address ranges.
3. The two parity memories to be interleaved must be in the same backplane.

4.9 CSR ADDRESS SELECTION

The address of the CSR is hardwired in the range of 772100 to 772136. Jumpers W1 through W4 (refer the Figure 5-14 for jumper locations) determine the discrete address.



X = Bit values selected by Jumpers W4 – W1

CSR ADDRESS

Table 4-4 shows the CSR addresses for all possible memory starting addresses and their jumper configurations. For example, if the lowest address memory responds to is 28K, the jumpers are cut for address 772110. If the lowest address memory responds to is 32K, the jumpers are also cut for address 772110. This is because the CSR addresses are assigned on a basis of 8K of memory. Thus, there are 16 unique addresses in the table.

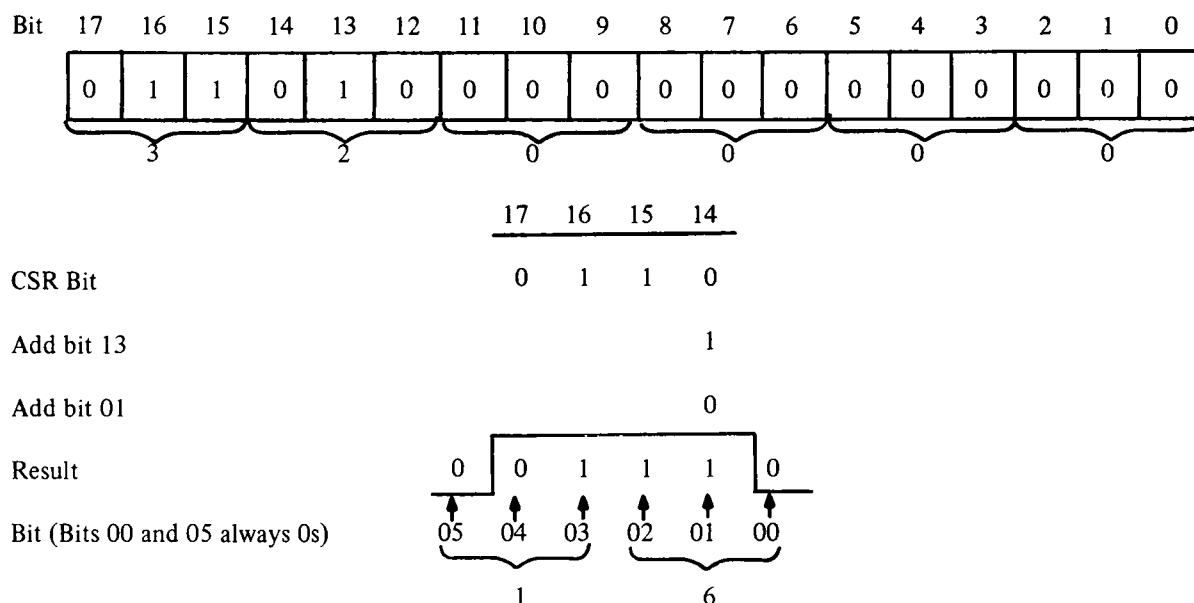
Table 4-4 CSR Address Jumper Selection for M7259 Parity Controller Module
Etch Rev D, CS Rev E

CSR Jumpers		W4	W3	W2	W1
Bus Address Line		A04	A03	A02	A01
Lower Memory Boundary	CSR Address				
0	772100	X	X	X	X
4K	772102	X	X	X	O
8K	772102	X	X	X	O
12K	772104	X	X	O	X
16K	772104	X	X	O	X
20K	772106	X	X	O	O
24K	772106	X	X	O	O
28K	772110	X	O	X	X
32K	772110	X	O	X	X
36K	772112	X	O	X	O
40K	772112	X	O	X	O
44K	772114	X	O	O	X
48K	772114	X	O	O	X
52K	772116	X	O	O	O
56K	772116	X	O	O	O
60K	772120	O	X	X	X
64K	772120	O	X	X	X
68K	772122	O	X	X	O
72K	772122	O	X	X	O
76K	772124	O	X	O	X
80K	772124	O	X	O	X
84K	772126	O	X	O	O
88K	772126	O	X	O	O
92K	772130	O	O	X	X
96K	772130	O	O	X	X
100K	772132	O	O	X	O
104K	772132	O	O	X	O
108K	772134	O	O	O	X
112K	772134	O	O	O	X
116K	772136	O	O	O	O
120K	772136	O	O	O	O

O = Jumper Removed

X = Jumper Installed

Example: Assume that a starting address of 52K (320000_8) is desired. The example illustrates how the CSR parity address is determined.



NOTE

When two 32K memories from different backplanes are interleaved, bit A01 is set for the minimum address in one 32K memory and is not set for the minimum address in the other 32K memory.

Address 16 is parity address 772116, since the upper four octal digits are hardwired as 7721XX₈ (Table 4-4). Consequently, for a 52K starting address, the corresponding CSR parity address is 772116 and jumpers W4, W3, and W2 are out (Table 4-4 – W1 is left intact).

When using the algorithm to determine the CSR addresses, one point should be kept in mind. It is assumed that the addresses the memory responds to are contiguous except for interleaving.

Table 4-5 shows the CSR address for each 4K increment of memory. For example, if the lowest address memory responds to is 32K, the parity register address is cut for 772110. If the lowest address memory responds to is 36K the parity register address is also cut for 772110. Consequently, the CSR addresses are assigned on a basis of 8K of memory. Thus, there are 16 unique CSR addresses as shown. The CSR addresses in the table assume the memories are not interleaved or are interleaved within the same backplane. With interleaved memories, the algorithm should be employed to determine the CSR address.

Table 4-5 CSR Addressing

Memory Start	Corresponding Parity Register Address
0	772100
4K	772102
8K	772102
12K	772104
16K	772104
20K	772106
24K	772106
28K	772110
32K	772110
36K	772112
40K	772112
44K	772114
48K	772114
52K	772116
56K	772116
60K	772120
64K	772120
68K	772122
72K	772122
76K	772124
80K	772124
84K	772126
88K	772126
92K	772130
96K	772130
100K	772132
104K	772132
108K	772134
112K	772134
116K	772136
120K	772136



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CHAPTER 5 INSTALLATION AND MAINTENANCE

5.1 INTRODUCTION

This chapter discusses the preventive and corrective maintenance procedures that apply to the MF11-W/WP Memory. A major point in the maintenance philosophy of this manual is that the user understand the normal operation of the memory as described in the previous chapters. This knowledge, plus the maintenance information included in this chapter, will aid the user in isolating and correcting malfunctions.

5.2 INSTALLATION

Paragraph 5.2.1 describes the mounting box and power requirements for installing the MF11-W/WP in various equipments. Paragraph 5.2.2 describes the selection of jumpers for the desired memory addressing and the jumper selection for interleaved and non-interleaved operation. The jumpers for the strobe margin and bias current are also described. Paragraph 5.2.3 is a step-by-step procedure for installing the MF11-W/WP as an add-on to an existing system.

5.2.1 Mounting Box and Power System

The MF11-W/WP must be installed in a mounting box capable of holding a PDP-11 double system unit with the facility of +20 V, -5 V, and +5 V power distribution and supplies.

The power distribution systems and cabinets for the PDP-11/40, PDP-11/35, PDP-11/45, PDP-11/50, and the H960-D or -E cabinet with expander box have been revised. Figure 5-1 illustrates how the MF11-W/WP connects with the new revised power distribution system. Figure 5-2 illustrates how the MF11-W/WP connects with the earlier power distribution system.

The MF11-W/WP cannot be used in the CPU cabinet of the earlier version of the PDP-11/45/50 and when the MF11-W/WP is used in the earlier version of either the PDP-11/40/35 or the H960-D/E, an FM11-U field modification kit must be used. When the MF11-W/WP is used in either the earlier or the new system, an H754 regulator must also be used. Each regulator can handle two MF11-W/WP backplanes. Table 5-1 lists each type of equipment and the machine serial numbers that use the new and the earlier power distribution systems. The H754 regulator is included as part of the FM11-U field modification kit, therefore it is not called out in the table when the kit is required.

Table 5-1 Machine Serial Numbers for New and Earlier
Power Distribution Systems

Equipment	Early System	New System
PDP-11/40/35	0 - 5999 FM11-U required	6000 and up H754 required
PDP-11/45/50	0 - 1999 MF11-W/WP can't be used	2000 and up H754 required
H960-D/E	0 - 6999 FM11-U required	7000 and up H754 required

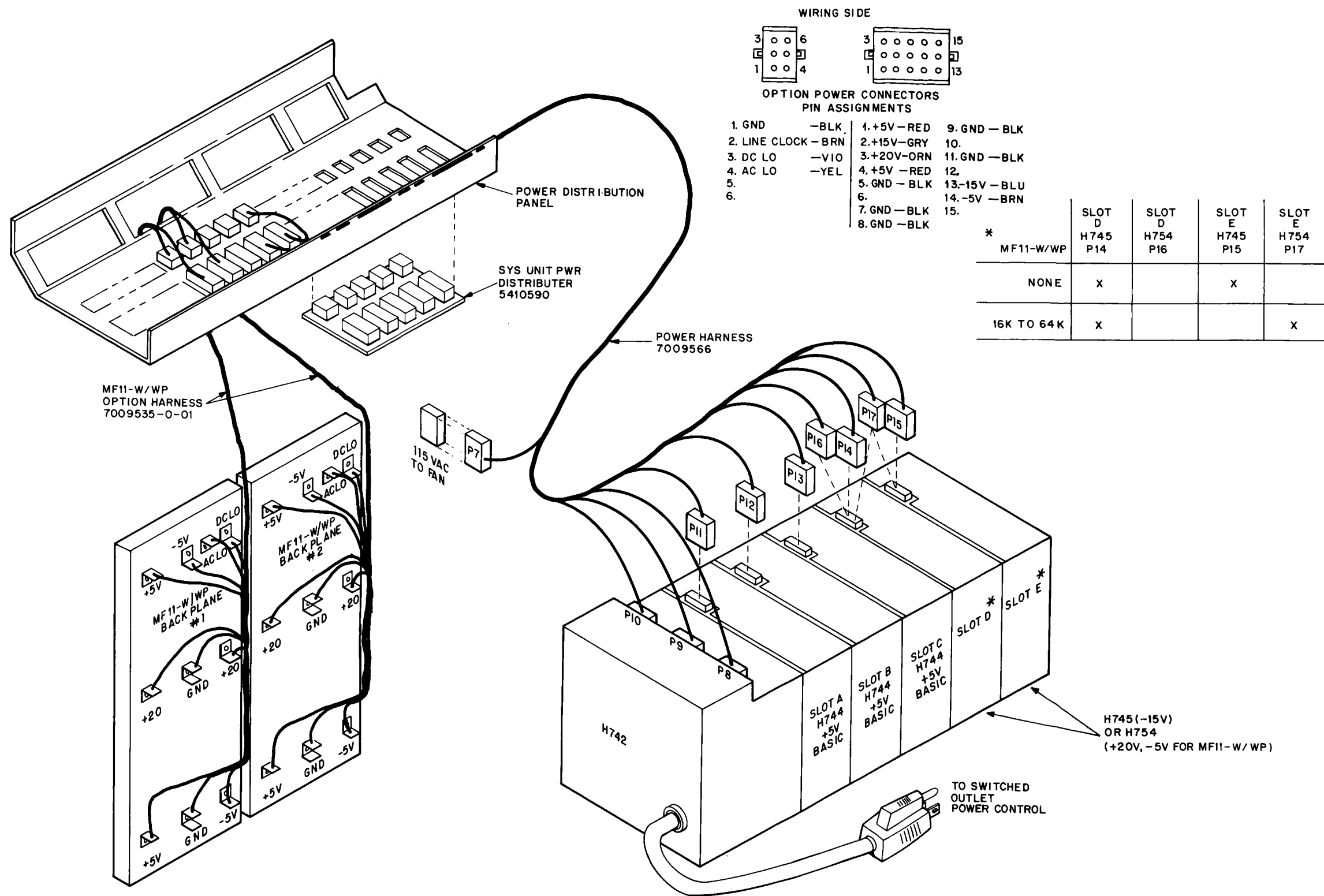


Figure 5-1 New MF11-W
Power Distribution System

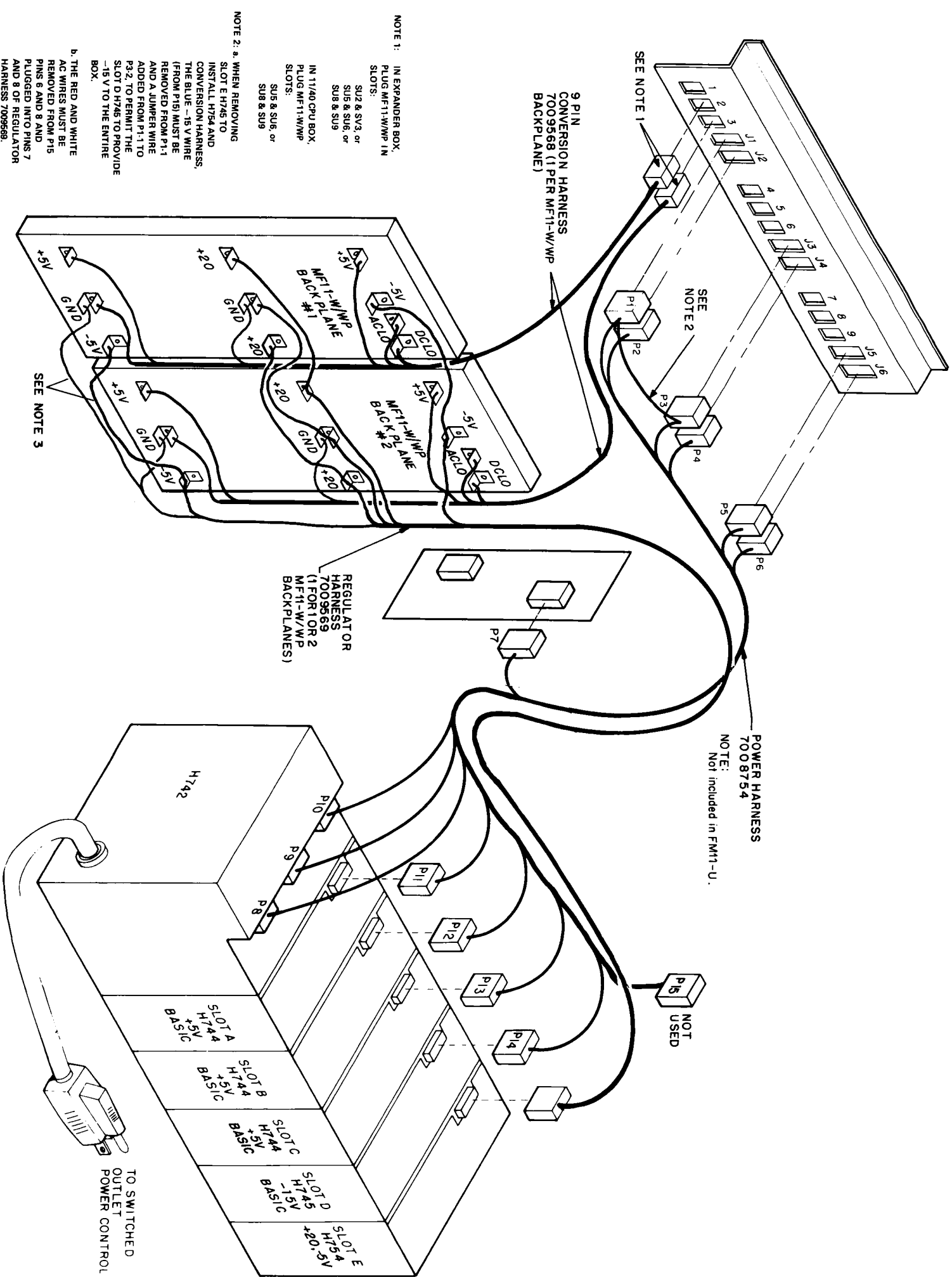


Figure 5-2 Early Power Distribution System for MF11-W/WP (With FM11-U Field Modification Kit)

The FM11-U includes a 7009569 conversion harness that must be used between the H754 +20 V, -5 Vdc regulator and the backplane, and a 7009568 harness which connects the backplane to the Power Distribution Panel (refer to Figure 5-2). One 7009569 harness can power two MF11-W/W/P backplanes. If only one is used, the jumpers between backplanes should be cut. One 7009568 harness is required per backplane.

The FM11-U field modification kit permits installation of up to two MF11-W/W/P backplanes of 32K memory. It consists of:

- 1 H754 regulator
- 1 7009569 regulator harness
- 2 7009568 9-pin conversion harness

Refer to the field modification kit print set (DD-FM11-U) for installation procedures.

5.2.2 MF11-W/W/P Backplane

Operation of the MF11-W or MF11-WP requires a 7009295-3 or 7009295-4 backplane, respectively. Upon installation of 32K core memory for field update from 16K core memory (backplane 7009295-1 or 7009295-2), the following wire connections are necessary to avoid backplane replacement. (These connections transform backplane 7009295-1 to 7009295-3 and backplane 7009295-2 to 7009295-4.)

F1P2 to F5J1

F9P2 to F6J1

E5J2 to E3J1

E6J2 to E8J1

These connections are made with 30 AWG wire by means of a wire wrap gun. (Note: 16K core memory, MM11-U, may still be used with the above wires installed.)

5.2.3 Jumpers Configuration

The M8294 32K Unibus Timing module and the G236 Driver module contain jumper wires. Tables 2-4 and 2-5 show the jumpers for selecting the device address and for selecting interleaved or non-interleaved operation. The address select jumpers are designated W3 through W7 and the interleaved jumpers are designated W1, W2, W8, W9, and W10 (Paragraph 2.4.3). Both sets of jumpers are located on the M8294 32K Unibus Timing module.

A second set of jumpers designated W1 through W7 is located on the G236 Driver module. Jumpers W1 through W4 (sheet DRVA) control the bias current. The cutting of jumpers on the G236 Driver module is a factory adjustment and should not be changed in the field. The strobe and bias current are set up at the factory with sophisticated test equipment.

The jumpers influence the parameters in a binary-weighted fashion. For the strobe margin, W2 has the least effect, W3 approximately twice the effect of W2, W4 twice the effect of W3, and W1 twice the effect of W4. For the bias current, W6 has the least effect, W7 has twice the effect of W6, and W5 has twice the effect of W7.

5.2.4 Installation Procedure

1. Unpack the MF11-W/WP and remove all packing material.
2. Locate the starting memory address by cutting jumpers W3 through W7 on the M8294 32K Unibus Timing module (Tables 2-4 and 2-5).
3. If interleaved operation is desired, change jumper wires W1, W2, W8, W9, and W10 as described in Paragraph 2.4.3.

CAUTION

Do not tamper with the jumper wires on the G236 Driver module. These jumpers are preset at the factory; any attempt to change them will result in reduced memory margins and reliability.

4. A backplane jumper is required from B1U1 to B2U1 for non-parity memory. This jumper should not be present for parity memory.
5. For the MF11-WP, ensure that jumpers W6 and W7 are installed on the M7259 Controller module. Jumpers W1, W2, W3, and W4 should be installed in accordance with Table 4-4.
6. Ensure that the H754 Regulator is installed in the H742 Power Supply, located in the 11/40 or 11/45 processor or expander cabinet. This regulator is necessary for proper operation of the MF11-W/WP. Additional information can be found in the *PDP-11/40 System Manual*, and the *PDP-11/45 and PDP-11/50 System Maintenance Manual*.
7. Ensure that the option power harness is properly connected between the power distribution panel and the backplane.
8. Install backplane assembly in processor mounting box or expander mounting box with four mounting screws.
9. Check backplane assembly for loose or damaged pins.
10. Perform a continuity check between the power supply outputs and ground to ensure that no output voltages are short-circuited.
11. Install modules in accordance with Module Utilization Chart shown in Figure 1-1. Ensure that the modules are firmly seated in the backplane assembly.

CAUTION

Use special care in positioning sense inhibit cables (flat, 40-conductor) to prevent pinching them when the drawer cover is closed. Avoid scraping cables with side two of the adjacent board as insulation damage may result.

NOTE

If only 32K of memory is to be installed, the modules may be placed in the left-half or the right-half of the backplane assembly. However, the modules must not be interspersed on both halves of the backplane, except for the M7259 Parity Controller, which is located in a fixed position in the backplane. This module should also be at revision E or later.

*NO - if only 32K
must be in left half
for AC/DC low
to be happy
Jan 2/11/80*

12. Connect the Unibus cable to the memory. If this is the last device on the bus, the Unibus should be terminated by inserting an M930 Unibus Terminator module in the BUS OUT slot. If this is not the last device of the bus, the Unibus should be continued by installing an M920 Unibus Jumper module or the BC11-A Unibus Cable to the BUS OUT slot.

NOTE

If the next device is in the same cabinet, the M920 Unibus Jumper module can be used.

13. Perform steps 1 through 9 of Paragraph 5.4.1, Voltage Adjustment Procedure.
14. In systems with parity, check and adjust the delay of the PCL SSYN DLY L signal as described in Paragraph 5.4.2.
15. Load and run all applicable diagnostic programs listed in this chapter. Verify that the program printout agrees with the total memory in the system.

NOTE

The pins listed in steps 16 through 20 are located on the G236 Driver module of the memory under test (either slot 5 or 6 on the backplane). The two resistors (470K ohm and 3.9K ohm) called out are included in the plastic components box of the MM11-W/WP Maintenance Repair Kit.

16. Halt the machine and connect a 470K ohm resistor between pin AU1 (G2360-0-1, sheet DRVA) and ground. This resistor allows high memory drive current. Load and run the 0-124K Memory Exerciser Diagnostic (MAINDEC-11-DZQMB) using pattern 1. Make two passes.
17. Halt the machine; disconnect the 470K ohm resistor from pin AU1, and connect it between pin AN2 and ground. This resistor allows low memory drive current. Run two passes of the DZQMB Diagnostic.
18. Halt the machine; disconnect the resistor from pin AN2 and connect a 3.9K ohm resistor between pin AV1 and ground. This resistor causes SENSE STROBE to occur early. Make two passes with the DZQMB Diagnostic.
19. Halt the machine; disconnect the 3.9K ohm resistor from ground and connect it between pin AV1 and +5 V. This causes SENSE STROBE to occur late. Make two passes with the DZQMB Diagnostic.
20. Halt the machine; disconnect the resistor and rerun the DZQMB Diagnostic to reverifi normal operation.

5.3 PREVENTIVE MAINTENANCE

Preventive maintenance consists of specific tasks performed at intervals to detect conditions that could lead to subsequent performance deterioration or malfunction. The following tasks are considered preventive maintenance items and are recommended to be performed every six months.

1. Visual inspection
2. Voltage measurements
3. Sense strobe delay check

4. Drive current check
5. PCL SSYN DLY check (for parity memories)
6. Strobe and drive current margins
7. MAINDEC testing

The two pieces of test equipment recommended for checking and troubleshooting the memory are the Tektronix 453 Dual Trace Oscilloscope or equivalent, and the Weston Schlumberger Model 4443 Digital Voltmeter or equivalent, with 0.5 percent accuracy.

CAUTION

Make sure all power is off before installing or removing modules. Use special care in positioning sense inhibit cables (flat, 40-conductor) to prevent pinching them when the drawer cover is closed. Avoid scraping cables with side two of the adjacent board as insulation damage may result.

5.3.1 Visual Inspection

Visually inspect the modules and backplane for broken wires, connectors, or other obvious defects.

NOTE

All tests and adjustments must be performed in an ambient temperature range of 20 degrees to 30 degrees C (68 degrees to 86 degrees F.)

5.3.2 Voltage Measurements

Turn on the primary power and measure the +20 V, +5 V, and -5 V at the option backplane. All voltages must be within ± 5 percent tolerance.

5.3.3 Sense Strobe Delay Check

To check sense strobe delay, connect channel A of the scope to pin FS1 and channel B to pin CN2 of the G236 Driver module. The correct delay is 160 ns ± 20 percent after the X read driver (FS1) turns on. Measure the delay from the 5 V point on the falling edge of the waveform at FS1 to the 1.5 V point on the falling edge of the waveform at CN2 as shown in Figure 5-3.

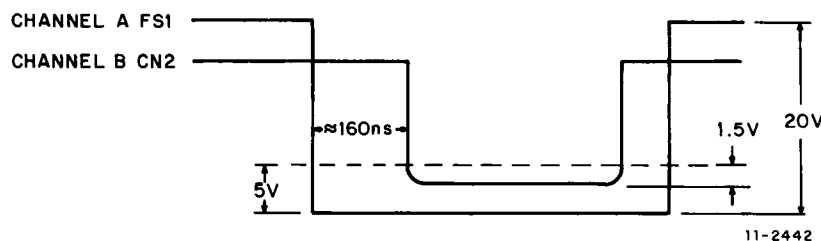


Figure 5-3 Sense Strobe Delay Waveform

5.3.4 Drive Current Checks

Connect a digital voltmeter (Weston Schlumberger Model 4443 or equivalent) between pin AK2 and +5 V on the G236 Driver module associated with the 32K memory being tested. The drive current is factory-set to provide appropriate drive margins and results in a voltage measurement of 365 mV ± 15 percent below the +5 V at 25° C (78° F).

5.3.5 PCL SSYN DLY Check (For Parity Memories Only)

Perform steps 1 through 3 of the adjustment procedure in Paragraph 5.4.3.

5.3.6 Strobe and Drive Current Margins

Perform steps 15 through 20 of the Installation Procedure, Paragraph 5.2.4.

5.3.7 MAINDEC Testing

Load and run for a minimum of two passes all the applicable diagnostic programs listed in Paragraph 5.5. No errors are permitted.

5.4 CORRECTIVE MAINTENANCE

This paragraph describes various adjustment procedures for specific corrective maintenance. It also includes three aids for performing corrective maintenance: a troubleshooting chart, waveforms for the sense inhibit circuits, and waveforms for the drive circuits.

5.4.1 Voltage Adjustment Procedure

1. Power down the equipment.
2. Disconnect the load from the H754 Power Supply.
3. Power up the equipment.
4. Connect the digital voltmeter to the +20 V and -5 V outputs of the H754.
5. Adjust the +20 V potentiometer R17, located on the side of the H754, for a 25 V reading.
6. Connect the digital voltmeter between the -5 V output and ground.
7. Adjust the -5 V potentiometer R21, located on the top of the H754, for -5 V. This procedure is necessary because the +20 V potentiometer sets the overall output of the regulator (25 V from +20 V to -5 V), while the -5 V adjustment controls the -5 V to ground output. Refer to schematic drawing D-CS-H754-0-1.
8. Power down and then reconnect the load.
9. Power up, recheck the voltages at the option backplane, and if necessary, adjust the outputs again.

5.4.2 Sense Strobe Delay and Drive Current Adjustments

Correction of any failure in either the sense strobe delay or drive current circuits on the G236 module that would require reconfiguration of the jumpers within these circuits should *not* be attempted in the field. Replace the faulty module with a spare G236 module and return the faulty G236 module to the factory for repair.

5.4.3 PCL SSYN DLY L Adjustment Procedure

This adjustment, for systems with parity, sets a 135-ns delay from the leading edge of SSYN INT BUS L to allow sufficient settling time for the parity checking logic. Too long a delay will result in increased cycle time and access time.

1. Load a branch dot instruction with a 000 777 format into an even address within the addressing range of the MF11-WP backplane being checked.
2. Connect channel A of the dual-trace scope to pin B02U1 and channel B to pin A02S2 of the M7259 module.

3. The delay from the 1 V point on the falling edge of the SSYN INT BUS L waveform to the 1 V point on the rising edge of the PCL SSYN DLY L waveform should be 135 ns as shown in Figure 5-4.
4. Adjust R16 on the M7259 module for 135-ns delay.

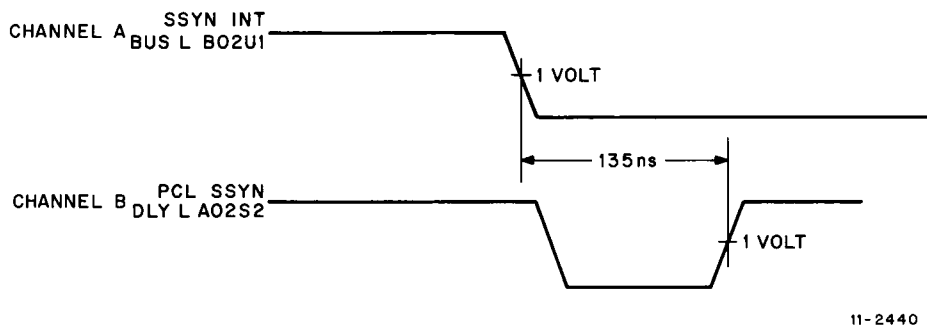


Figure 5-4 SSYN DLY L Timing Waveform

5.4.4 Corrective Maintenance Aids

Figure 5-5 is a troubleshooting chart arranged as a 2-axis grid that identifies fault versus location. Figure 5-6 shows the sense/inhibit circuitry and Figure 5-7 shows the various waveforms associated with the sense/inhibit circuitry. The encircled letters in Figure 5-6 are keyed to the waveforms in Figure 5-7. The drive circuitry is shown in Figure 5-8 and the associated waveforms are shown in Figure 5-9. The encircled letters in Figure 5-8 are keyed to the waveforms indicated in Figure 5-9. Figures 5-10 through 5-13 show the component layout of the MF11-W modules and designate the various functional groupings. Figure 5-14 shows the M7259 Parity Control module employed with the MF11-WP.

The waveforms are taken in the DATI and DATO modes with worst case memory patterns. They are representative of waveforms taken while running the 0-124K exerciser (DZQMB) with a starting location of 200. Signal MATB A EARLY L at pin CK1 of the M8294 module can be used as a sync signal for the scope. Minor variations in the waveforms may be observed between different memory systems.

5.5 MAINDEC TESTING

Certain DEC programs can be used to test various memory operations as an aid to troubleshooting. The purpose of each of these memory-related test programs, as well as the program abstract, is given in the following paragraphs. Each program contains instructions for use.

5.5.1 0-124K Memory Exerciser (MAINDEC-11-DZQMB)

The purpose of the 0-124K Memory Exerciser program is to test contiguous memory addresses from 000000 to 757776. It verifies that each address is unique (address test) and that each memory location can be read or written reliably (worst case noise test). If Memory Management is available, all testing is performed with Memory Management enabled (unless disabled). This program may be used to adjust/margin memory.

5.5.2 0-124K Memory I/O Exerciser (MAINDEC-11-DZQMA)

The purpose of the 0-124K Memory I/O Exerciser is to test sequentially all locations of core memory, or any 4K section of core memory, using any NPR device specified. The program checks bank selection, effective address bits, and memory. It can run stand-alone or with a Memory Management device to access extended memory. Worst case noise patterns are used with the NPR device to test memory. Printouts of NPR device errors are provided and include designation of the device under test, the content of its control and status register, and the content of its error register. Data error printouts include the address of the bad data, the true data sent, and the bad data received.

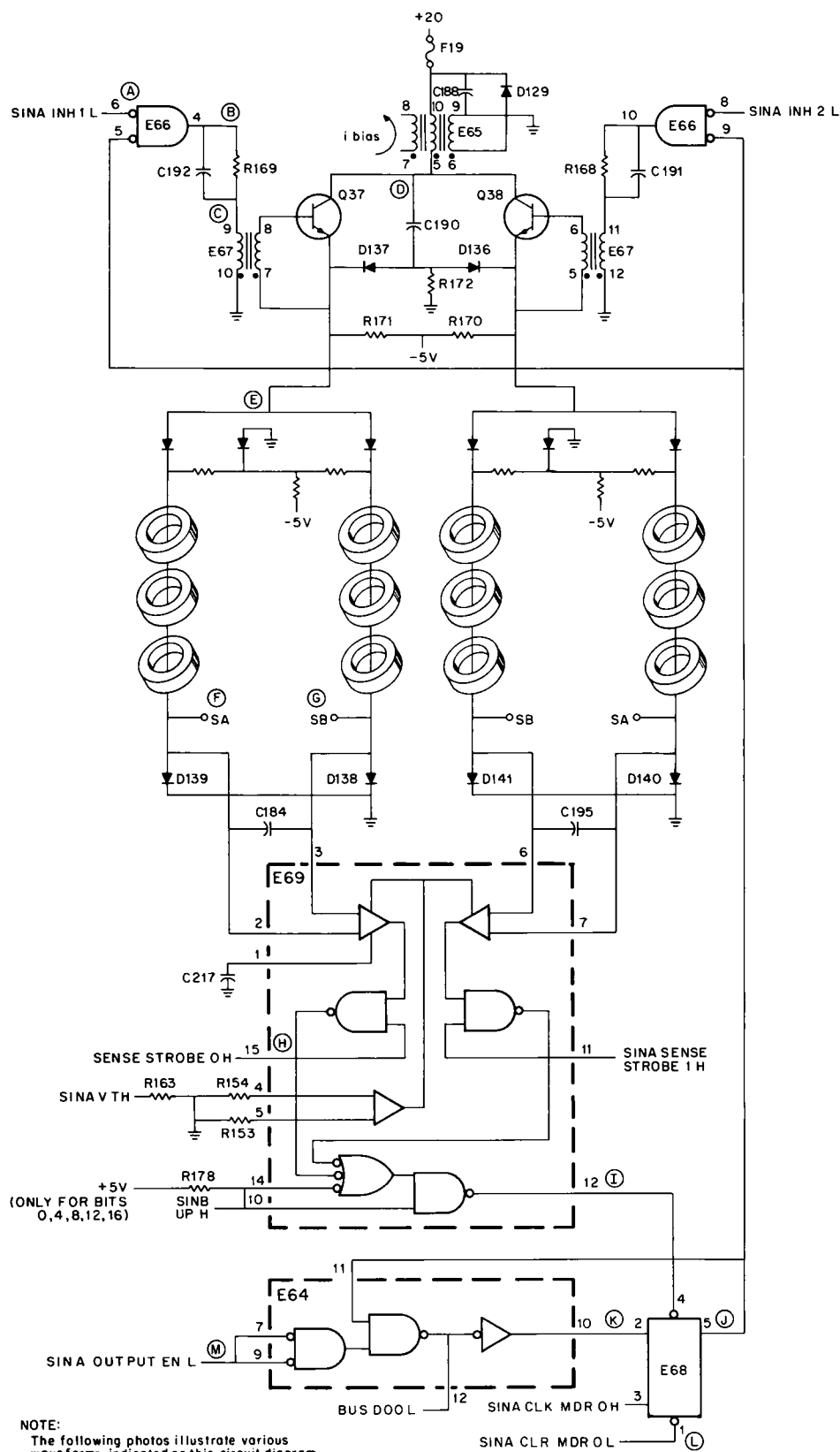


Figure 5-6 Typical Sense/Inhibit Circuit (D00)

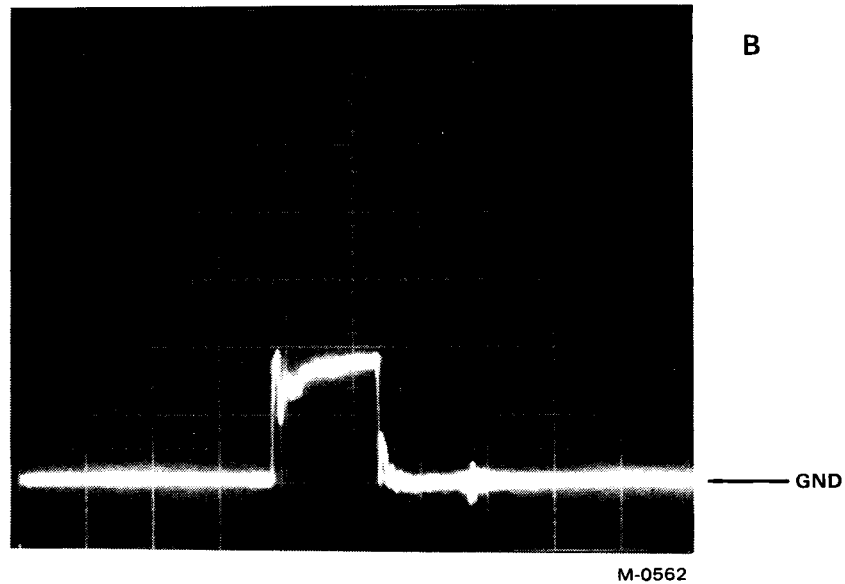
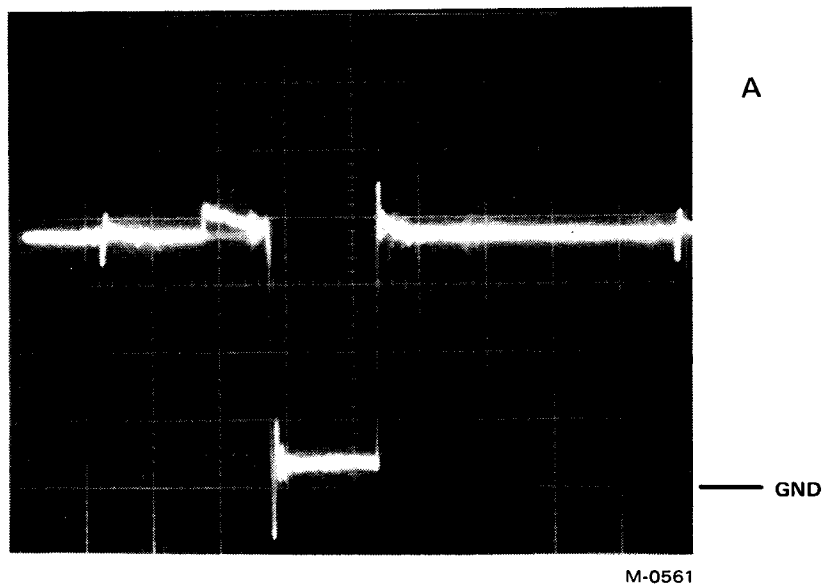


Figure 5-7 Sense Inhibit Module Waveforms (Sheet 1 of 6)

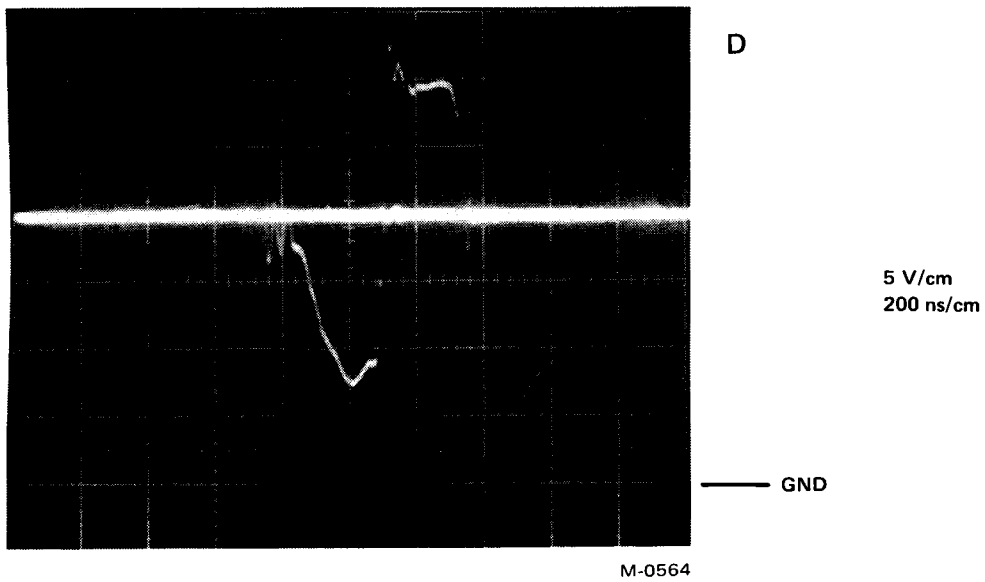
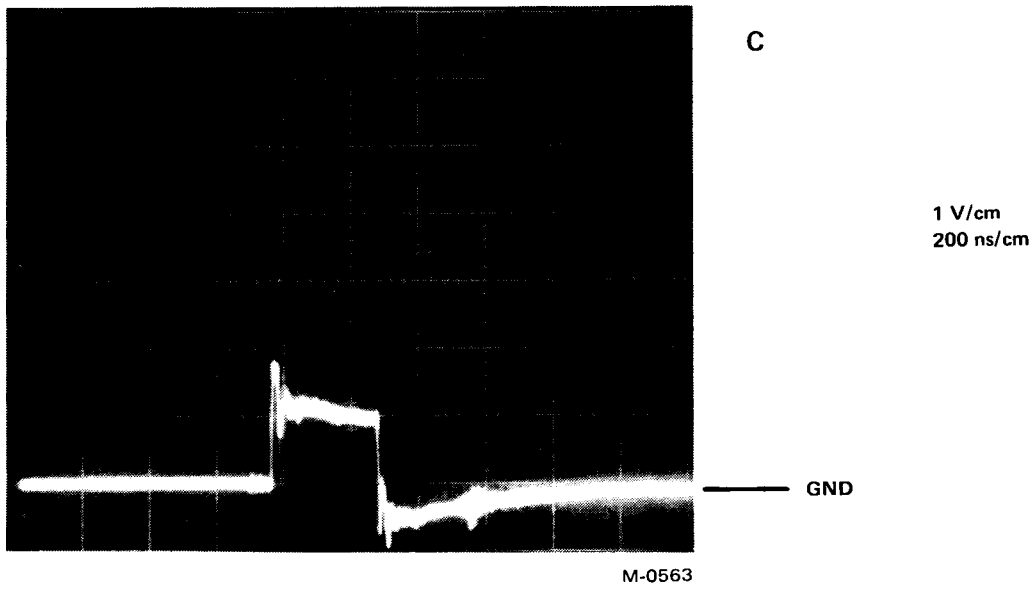


Figure 5-7 Sense Inhibit Module Waveforms (Sheet 2 of 6)

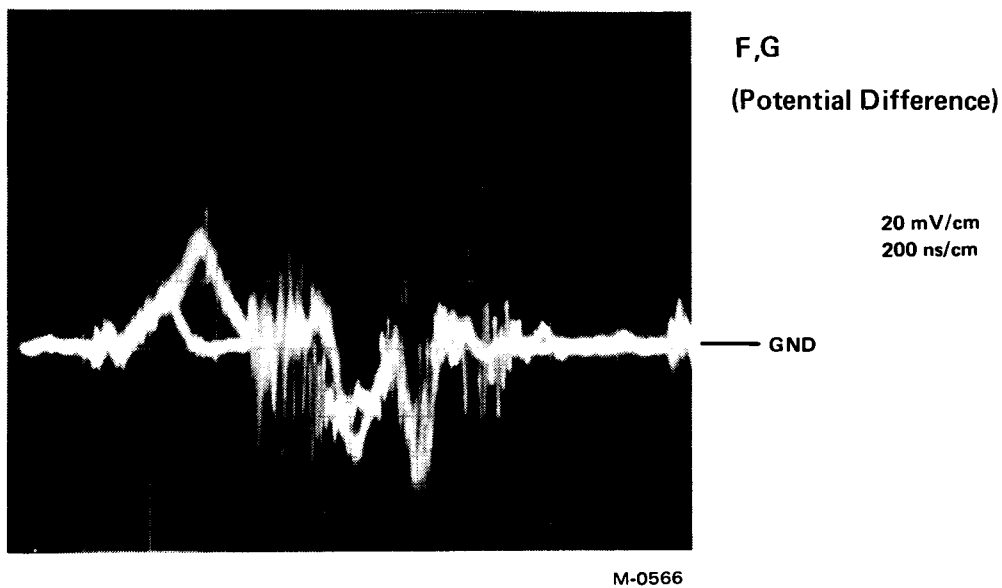
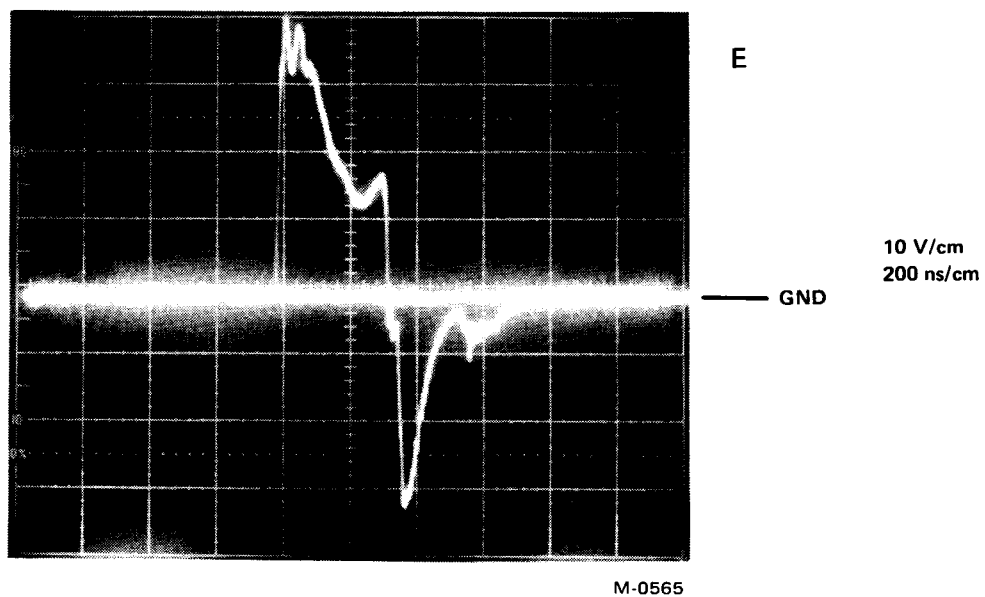


Figure 5-7 Sense Inhibit Module Waveforms (Sheet 3 of 6)

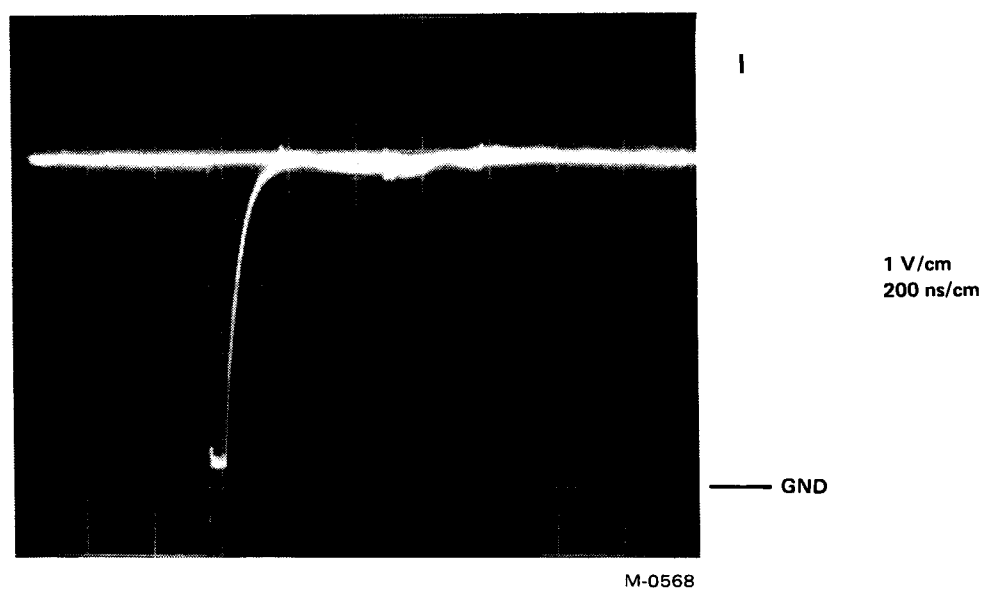
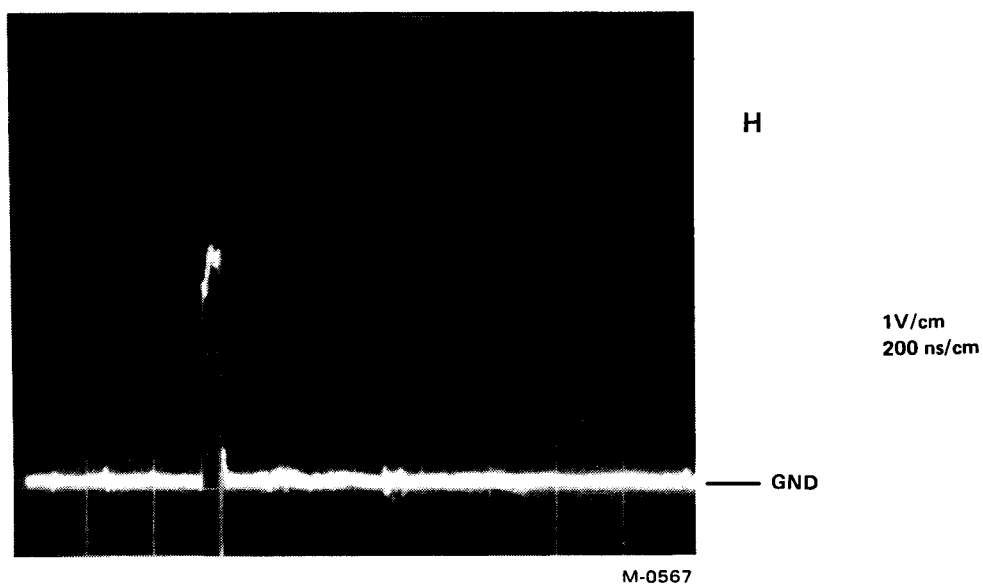


Figure 5-7 Sense Inhibit Module Waveforms (Sheet 4 of 6)

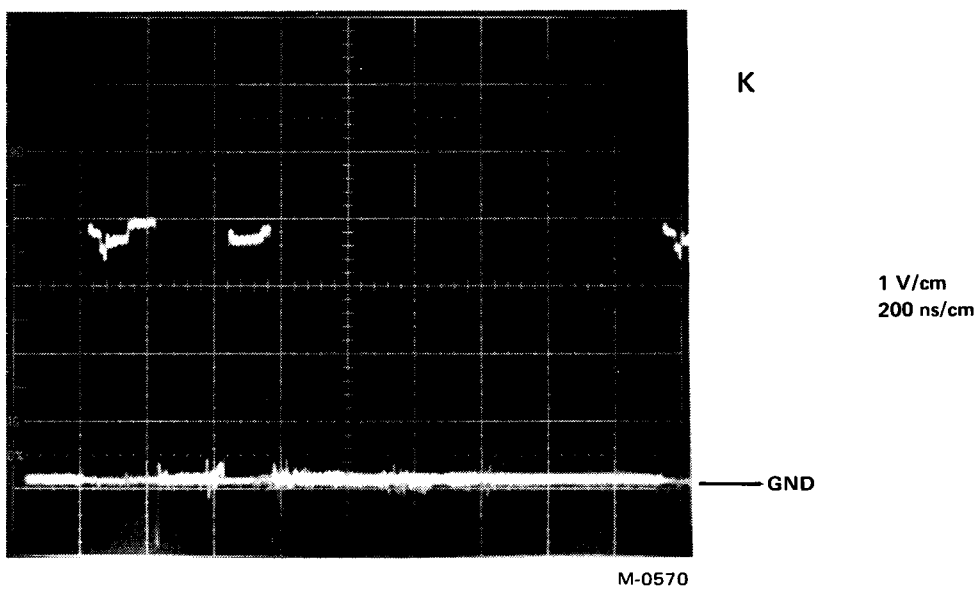
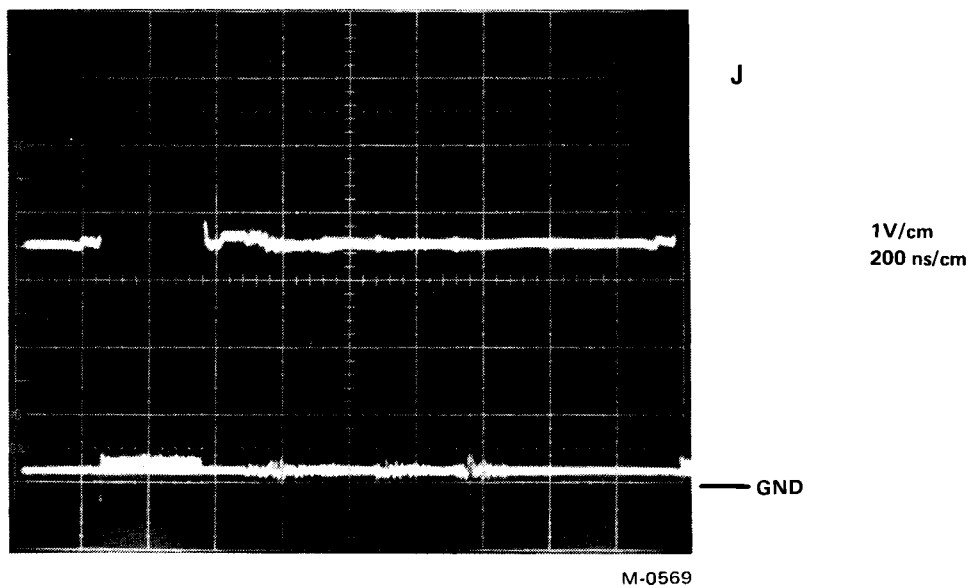
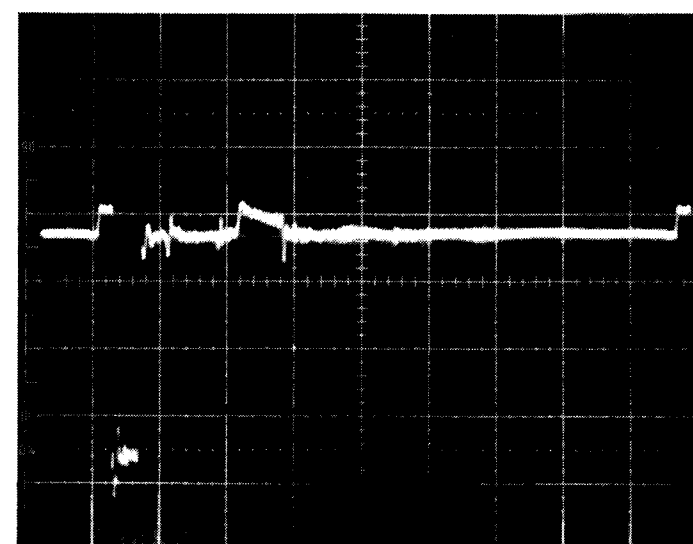


Figure 5-7 Sense Inhibit Module Waveforms (Sheet 5 of 6)

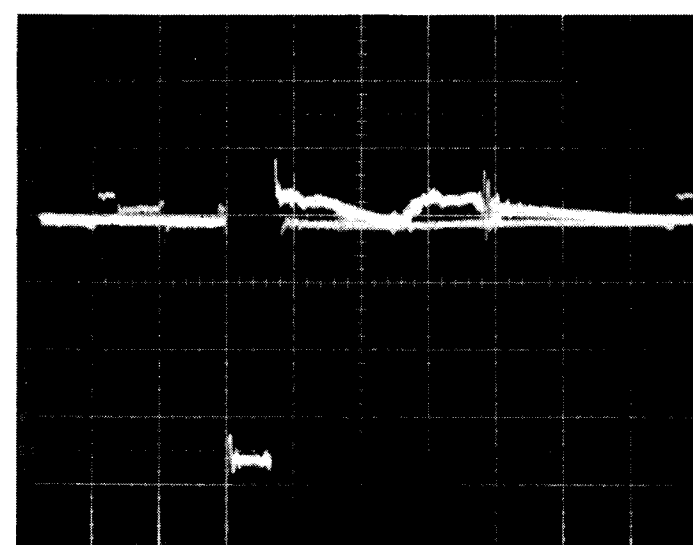


L

1 V/cm
200 ns/cm

GND

M-0571



M

1 V/cm
200 ns/cm

GND

M-0572

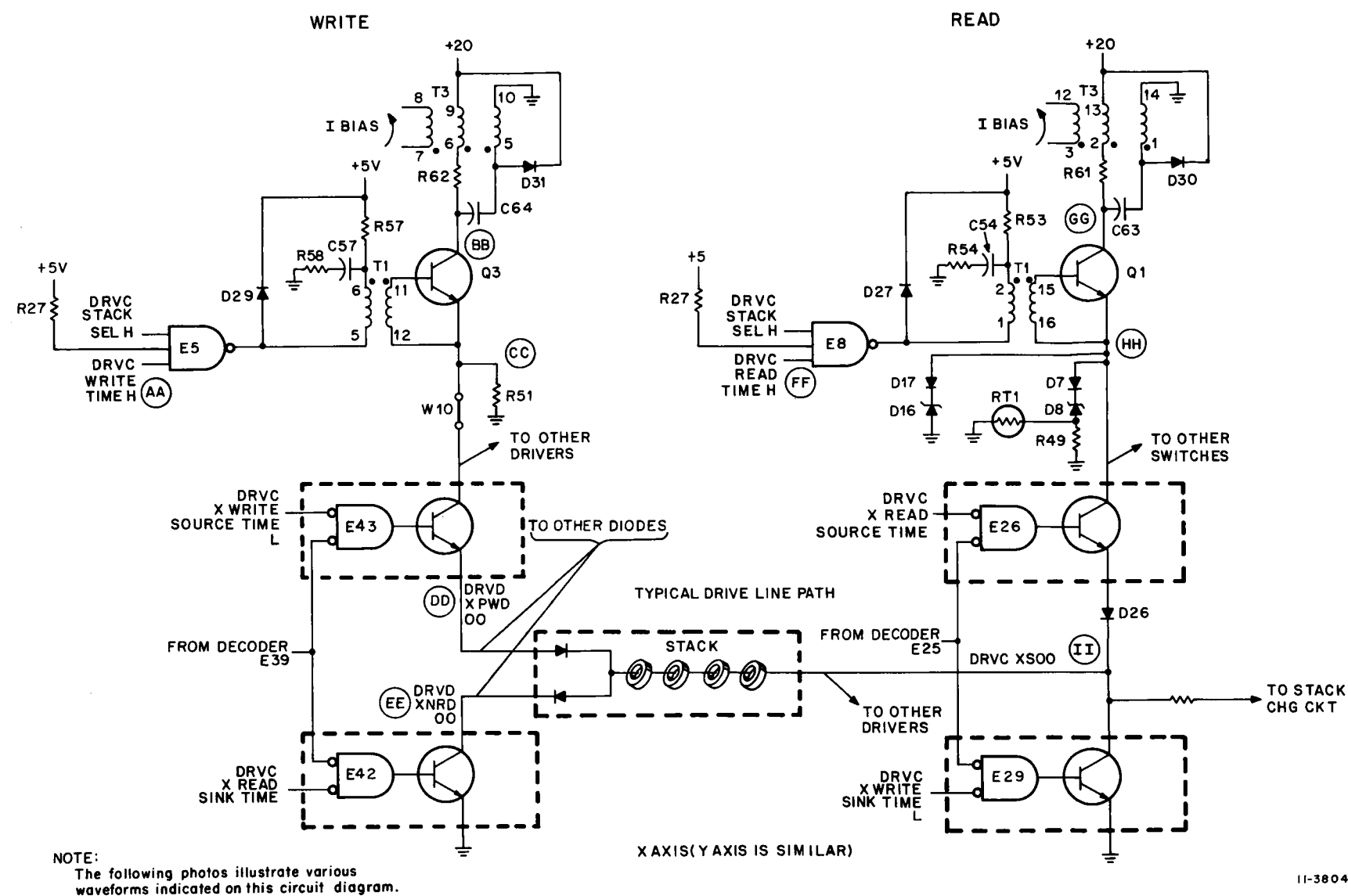


Figure 5-8 Typical Read/Write Drive Circuit

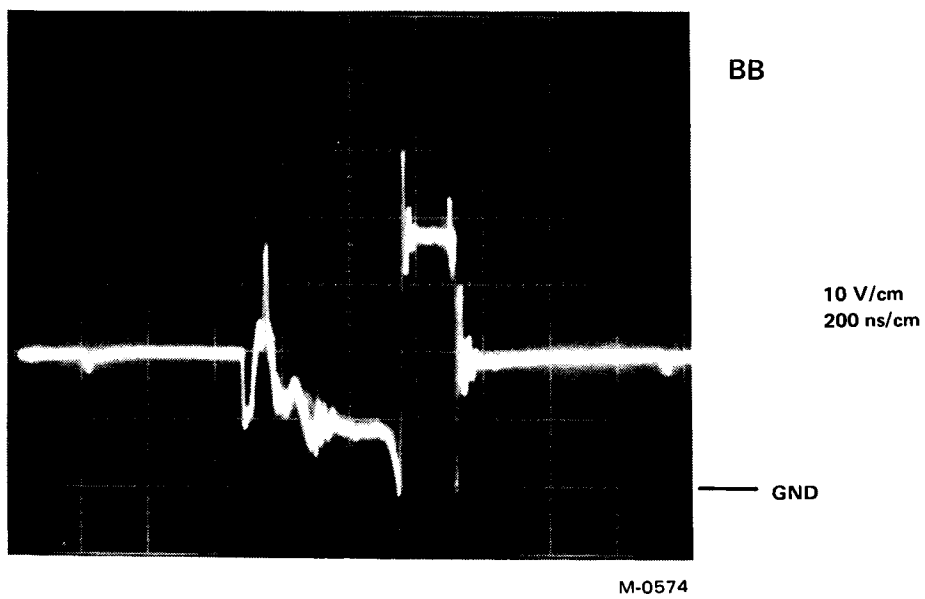
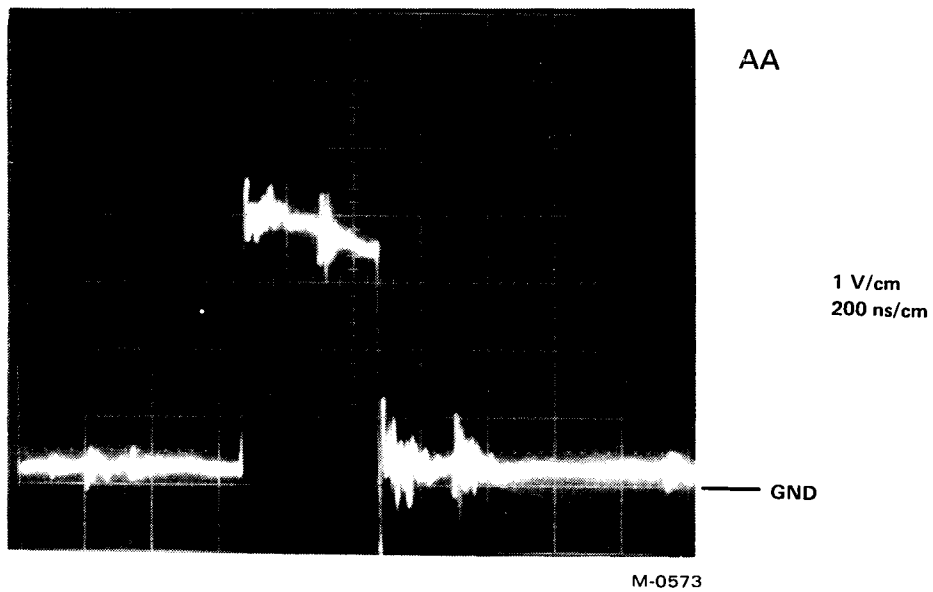


Figure 5-9 Drive Module Waveforms (Sheet 1 of 5)

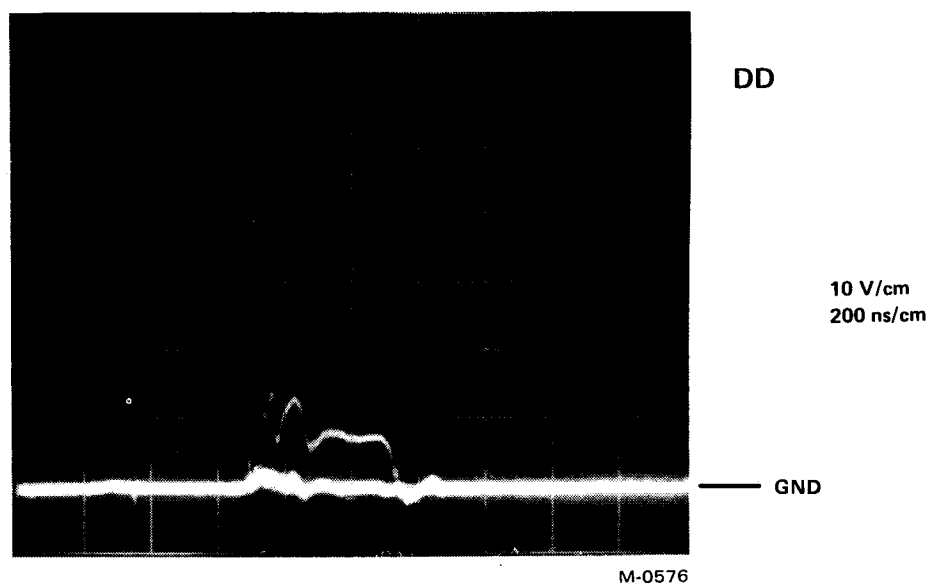
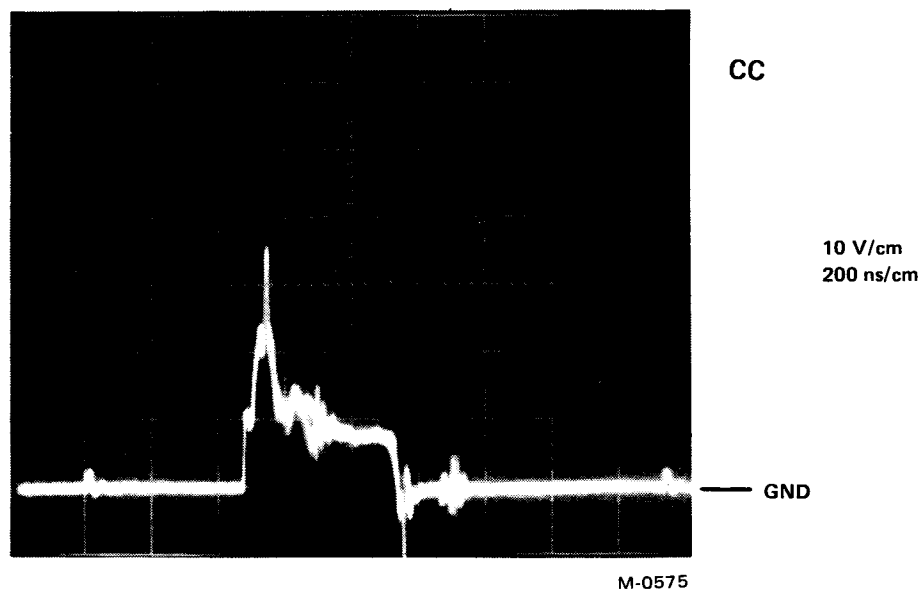


Figure 5-9 Drive Module Waveforms (Sheet 2 of 5)

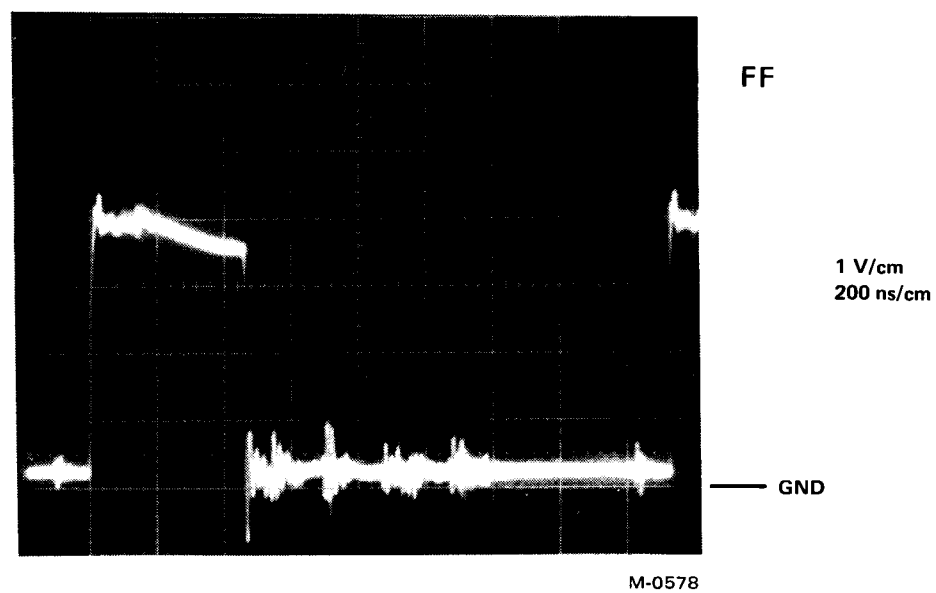
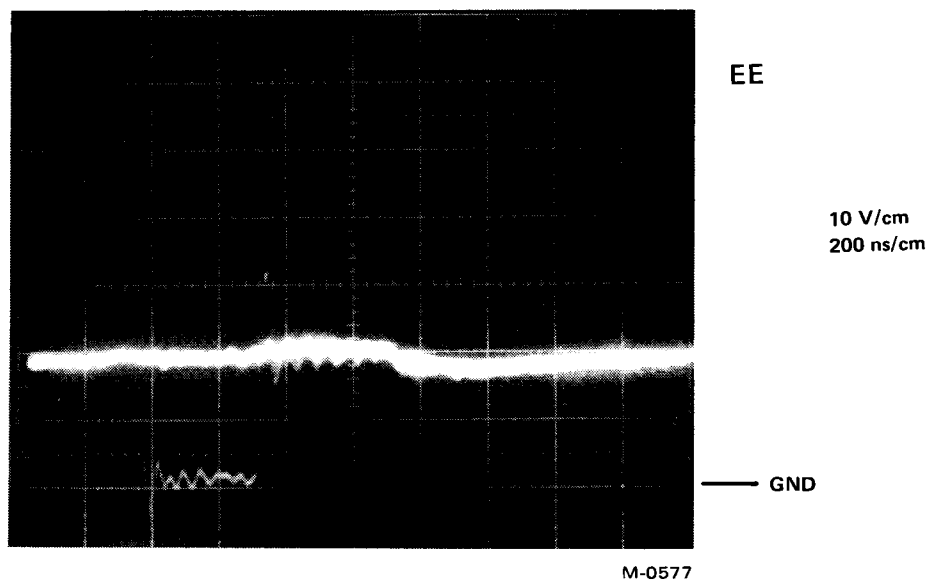
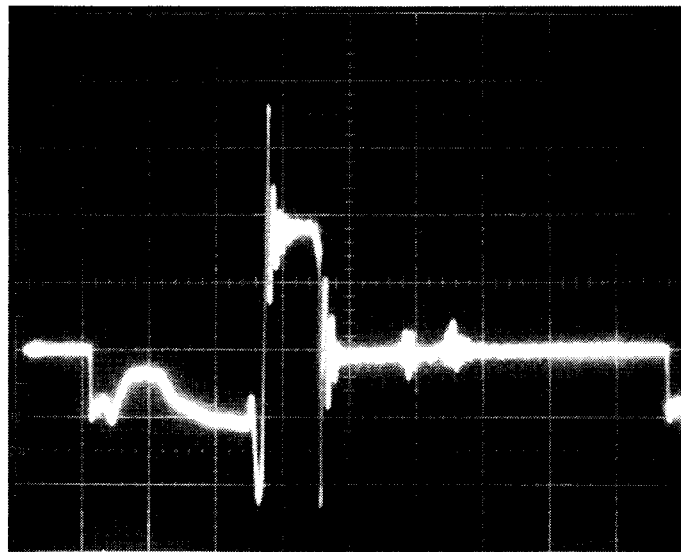


Figure 5-9 Drive Module Waveforms (Sheet 3 of 5)



GG

10 V/cm
200 ns/cm

— GND

M-0579



HH

10 V/cm
200 ns/cm

— GND

M-0580

Figure 5-9 Drive Module Waveforms (Sheet 4 of 5)

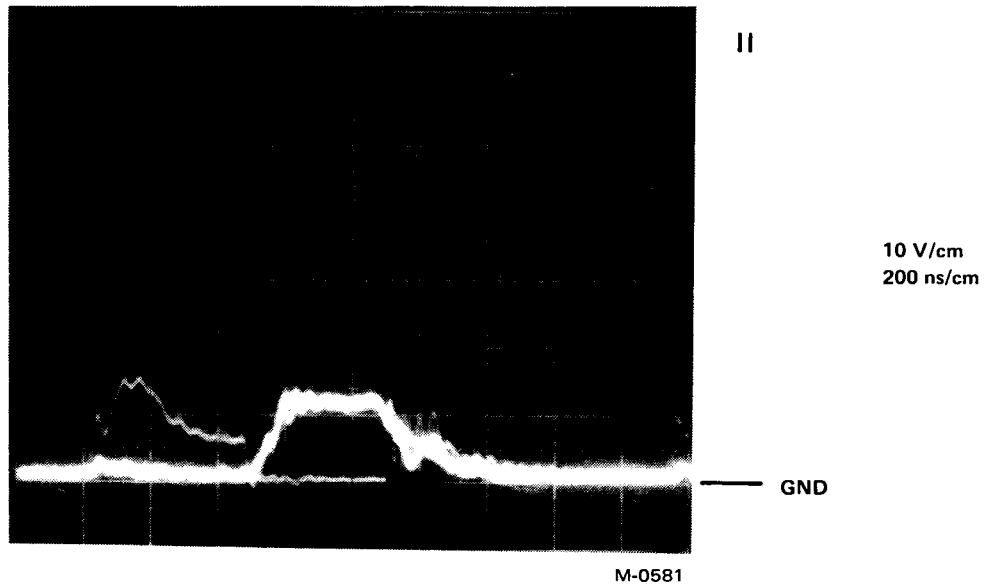
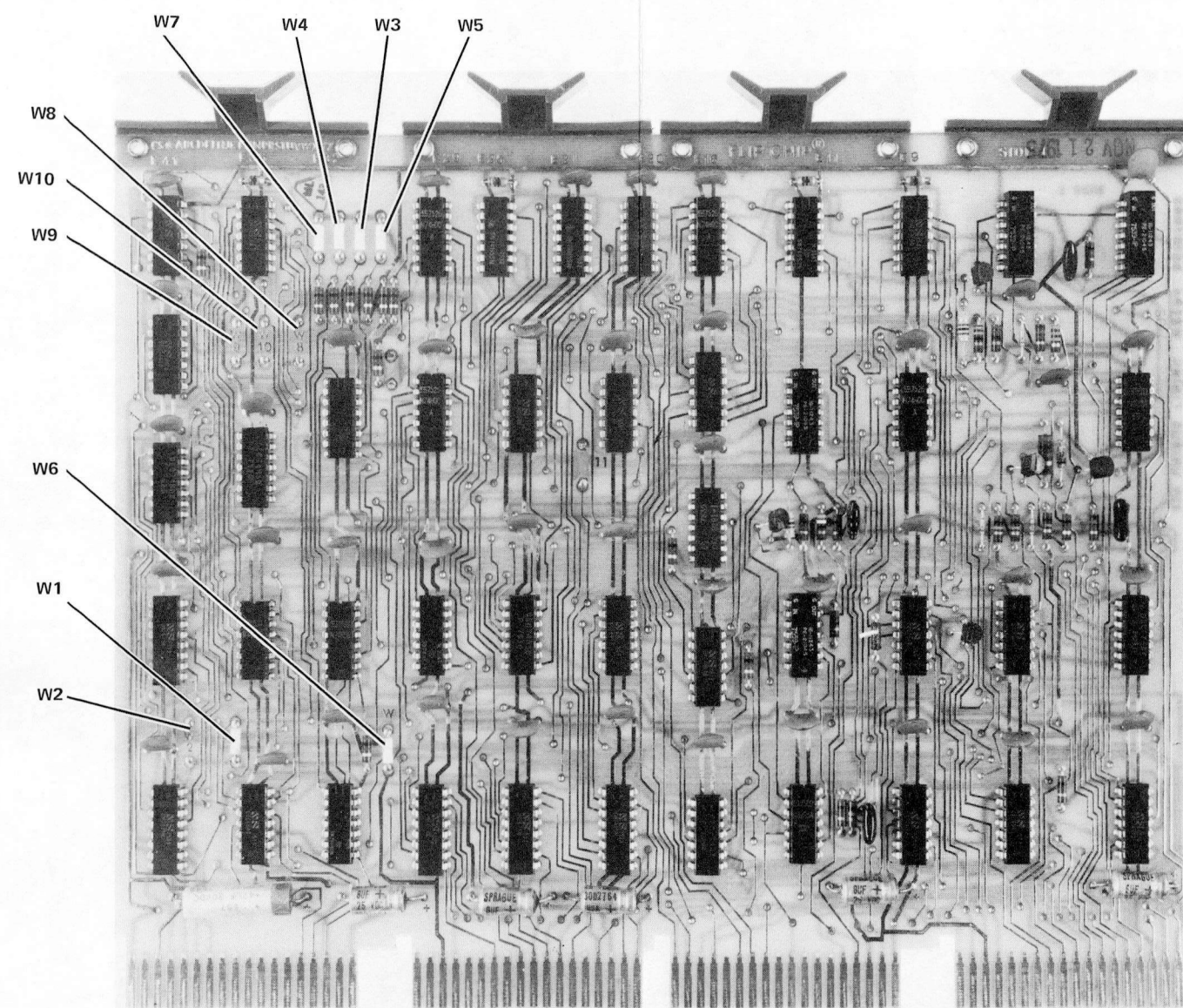


Figure 5-9 Drive Module Waveforms (Sheet 5 of 5)



NOTE: W1, W2, W8, W9, and W10 ARE SELECTED FOR INTERLEAVED OR NON-INTERLEAVED OPERATION. W3, W4, W5, W6, and W7 ARE SELECTED FOR STARTING ADDRESS REFER TO PRINT MATA FOR JUMPER CONFIGURATION

7870-2

Figure 5-10 M8294 32K Unibus Timing Module

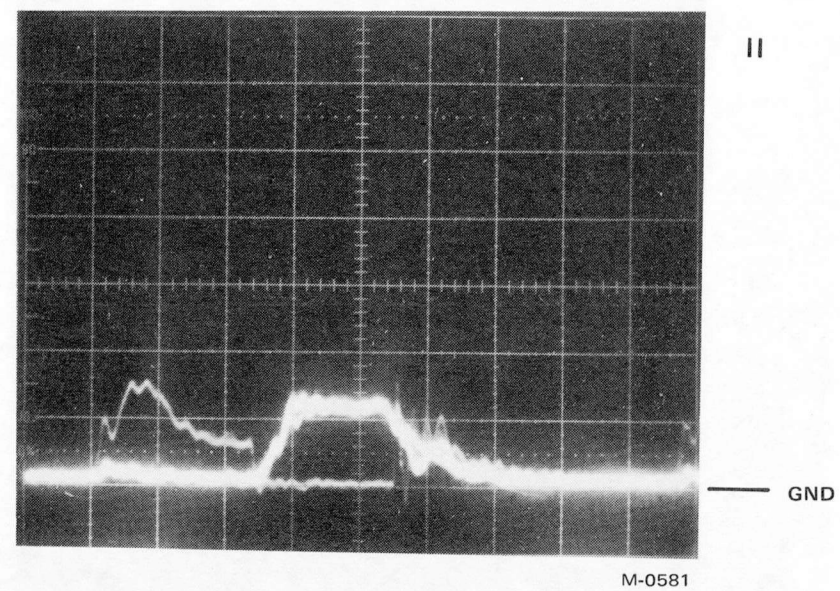


Figure 5-9 Drive Module Waveforms (Sheet 5 of 5)

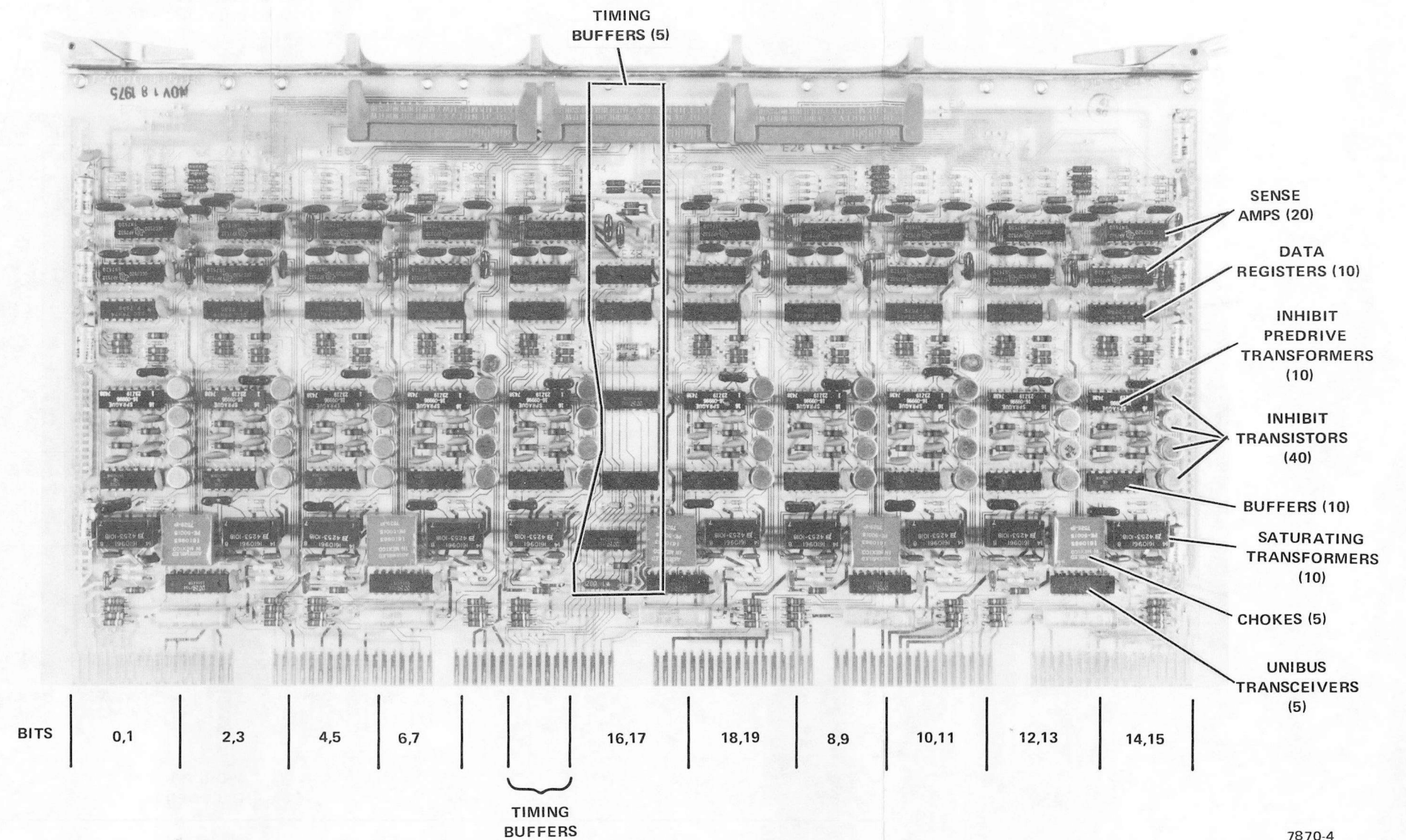
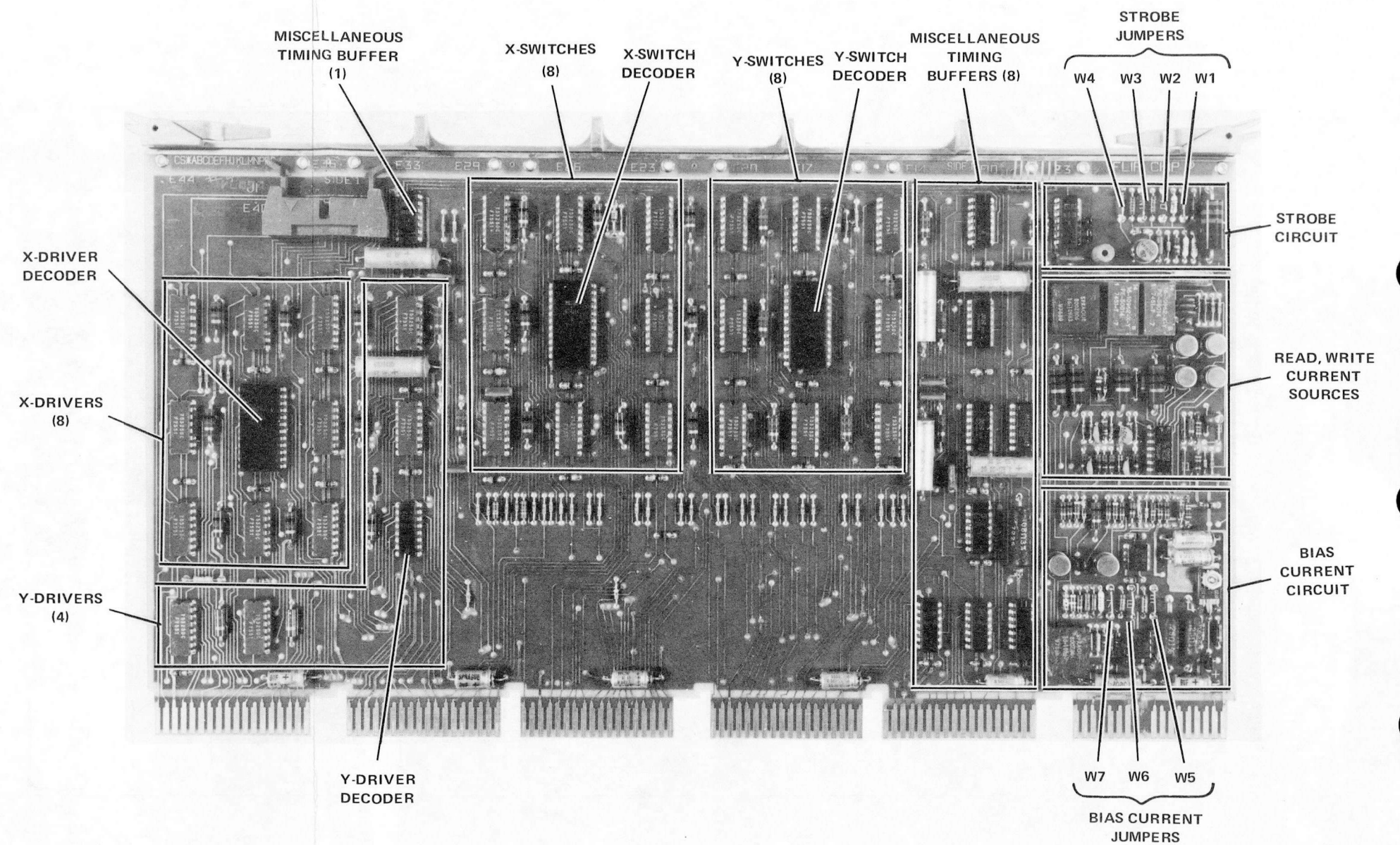
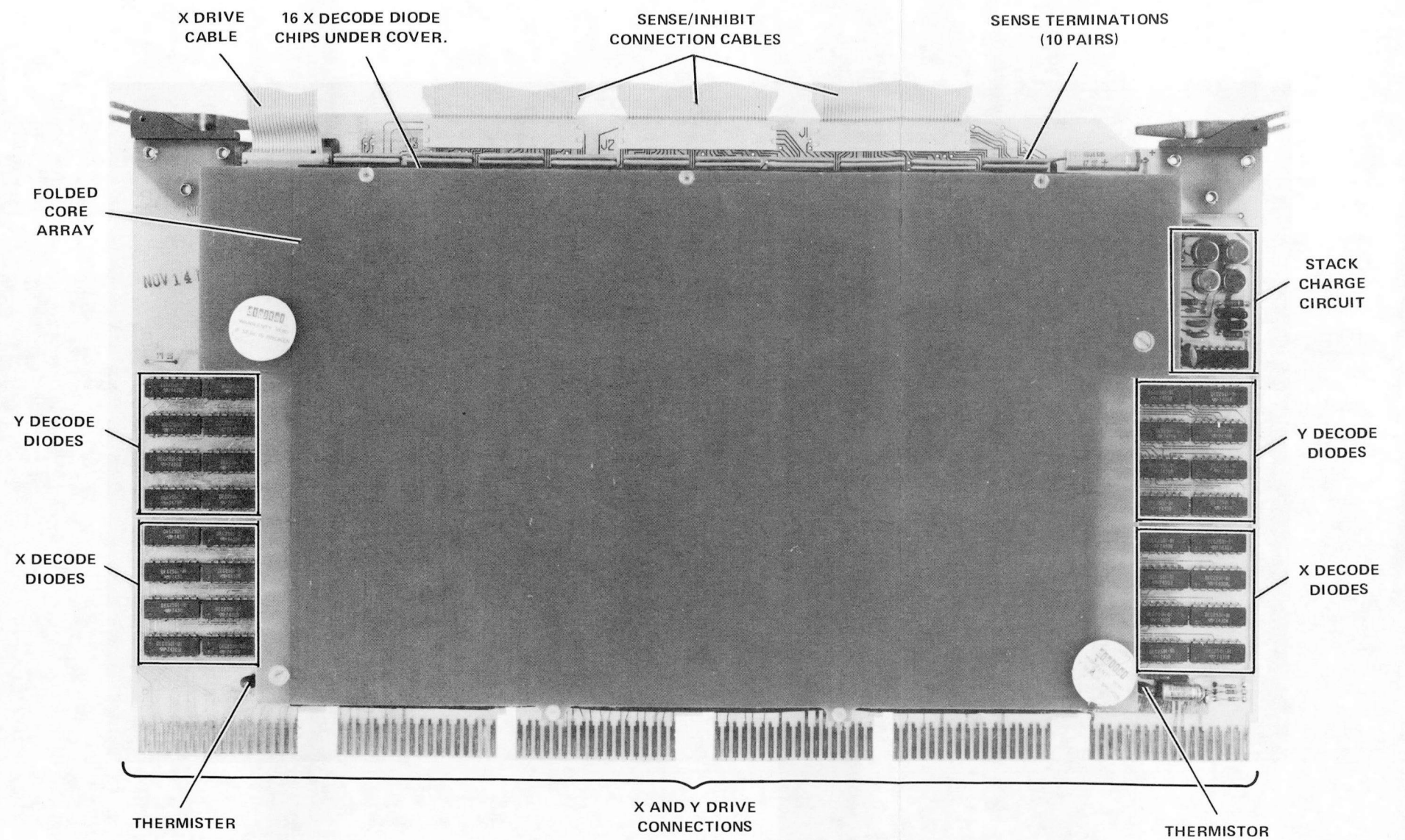


Figure 5-11 G116 Sense Inhibit Module



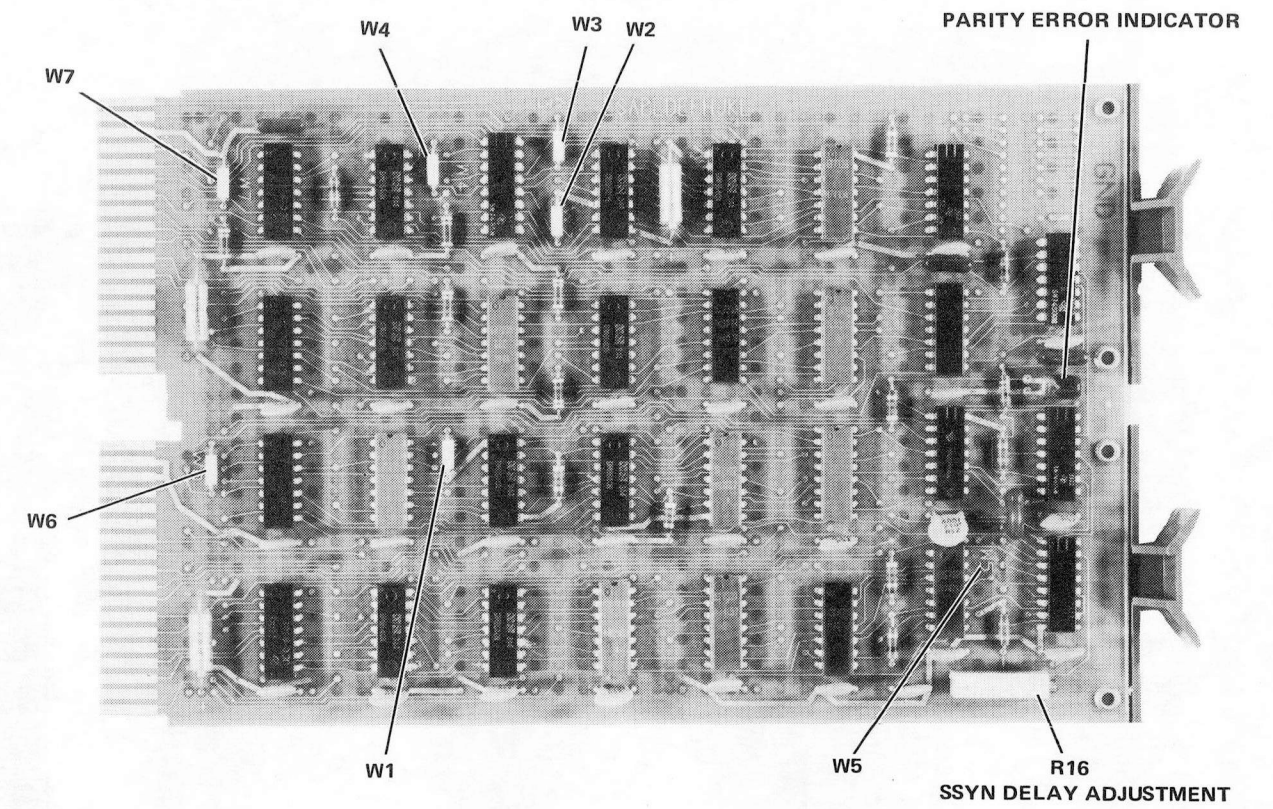
7870-1

Figure 5-12 G236 X-Y Driver Module



7870-3

Figure 5-13 H224 Stack Module



6927-1

Figure 5-14 M7259 Parity Control Module

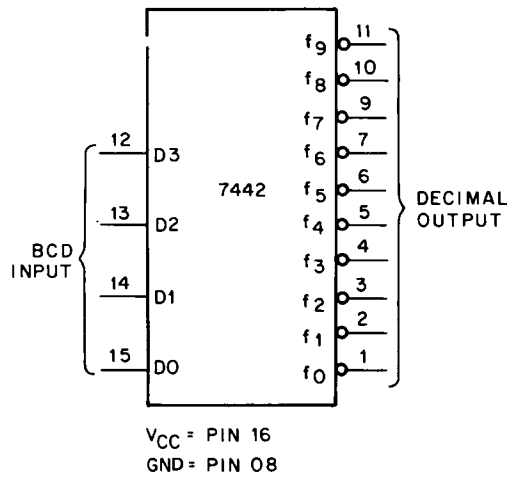
APPENDIX A IC DESCRIPTIONS

The following ICs are described in this appendix:

7442	4-Line to 1-Line Decoder
7475	4-Bit Bistable Latch
7483	4-Bit Binary Adder
7485	4-Bit Comparator
7520	Sense Amplifier
82S62	9-Bit Parity Generator and Checker
74121	Monostable Multivibrator
74154	4-Line to 16-Line Decoder

7442 4 LINE TO 1 LINE DECODER

These BCD-to-decimal decoders consist of eight inverters and ten 4-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates.



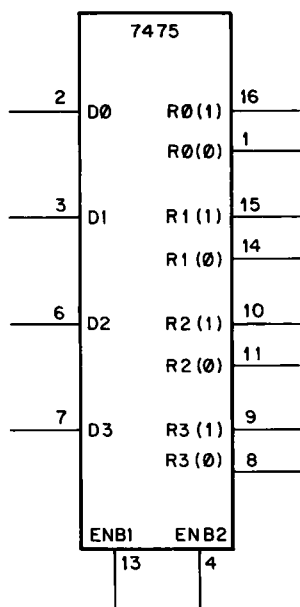
IC-7442

7442
TRUTH TABLE

BCD Input				Decimal Output									
D3	D2	D1	D0	f0	f1	f2	f3	f4	f5	f6	f7	f8	f9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

7475 4-BIT BISTABLE LATCH

The 7475 latches are used for temporary storage of binary information. Information present at a data (D) input is transferred to the R output when the clock is high, and the R output will follow the data input as long as the clock remains high. When the clock goes low, the information (present at the data input at the time of the transition) is retained at the R output until the clock is permitted to go high. Input ENB1 is the clock input for data inputs D0 and D1. ENB2 is the clock input for data inputs D2 and D3.



DN INPUTS		RN (1) OUTPUTS		CLOCK INPUTS
D0				
0	1	0	1	ENB1
D1	0	0	1	
D2	0	0	1	ENB2
D3	0	0	1	

VCC PIN 5
GND PIN 12

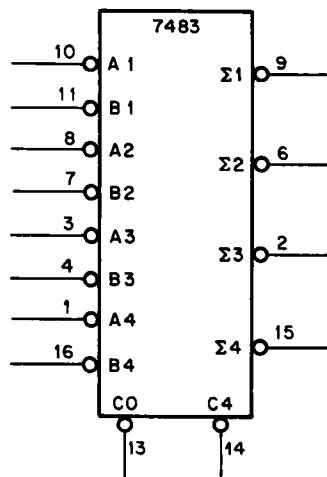
NOTE:

1. RN(0) Outputs = inverted RN(1) outputs.
2. ENB1 and ENB2 clock on negative going edge.

IC-7475

7483 4-BIT BINARY ADDER

The 7483 Binary Adder adds two 4-bit binary numbers. The sum outputs are provided for each bit and the resultant carry is obtained from the C_4 output.



VCC = PIN 5
GND = PIN 12

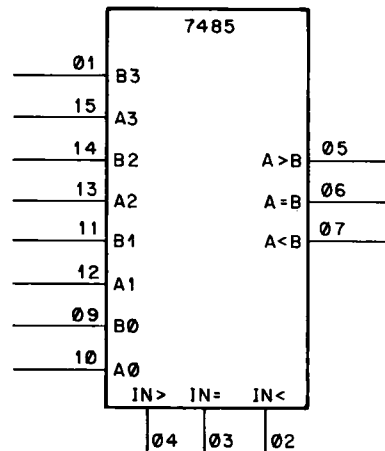
Note: If cascaded, $C_0 = C_4$ from preceding adder and $C_4 = C_0$ from succeeding adder.

				C_0
	A_4	A_3	A_2	A_1
+	B_4	B_3	B_2	B_1
	C_4	Σ_4	Σ_3	Σ_2
				Σ_1

IC-7483

7485 4-BIT COMPARATOR

The 7485 performs magnitude comparison of straight binary or straight BCD codes. Three fully decoded decisions ($A > B$, $A < B$, $A = B$) about two 4-bit words (A,B) are made and externally available at three outputs.



VCC = PIN 16
OND = PIN 08

TRUTH TABLE

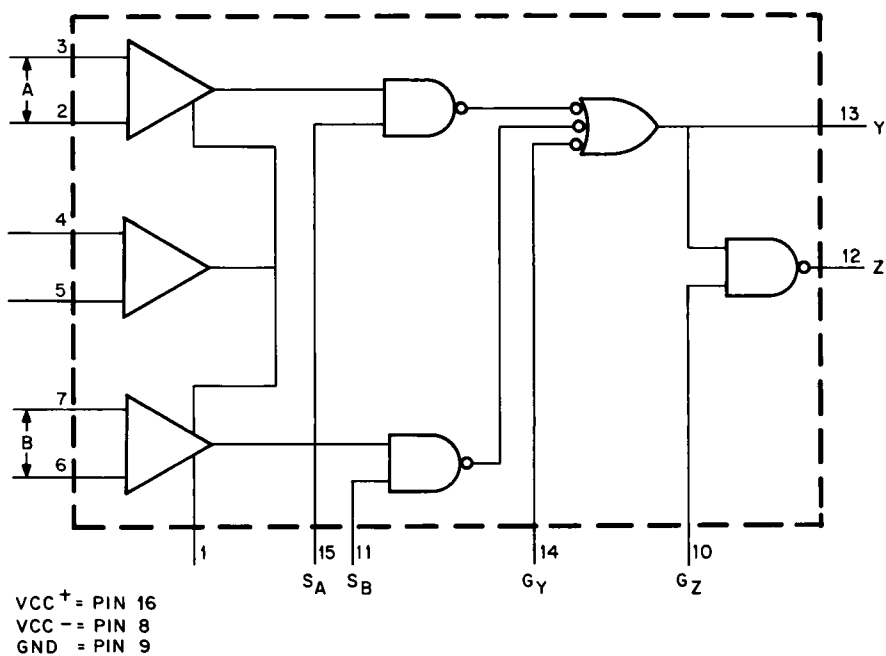
COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	IN >	IN <	IN =	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

IC-7485

7520 SENSE AMPLIFIER

The 7520 integrated circuit contains two dc-coupled, single preamplifier sense amplifiers and an OR gate to combine two separate data inputs. The two amplifiers are strobed separately, so only one of the two affects the output in any given cycle.



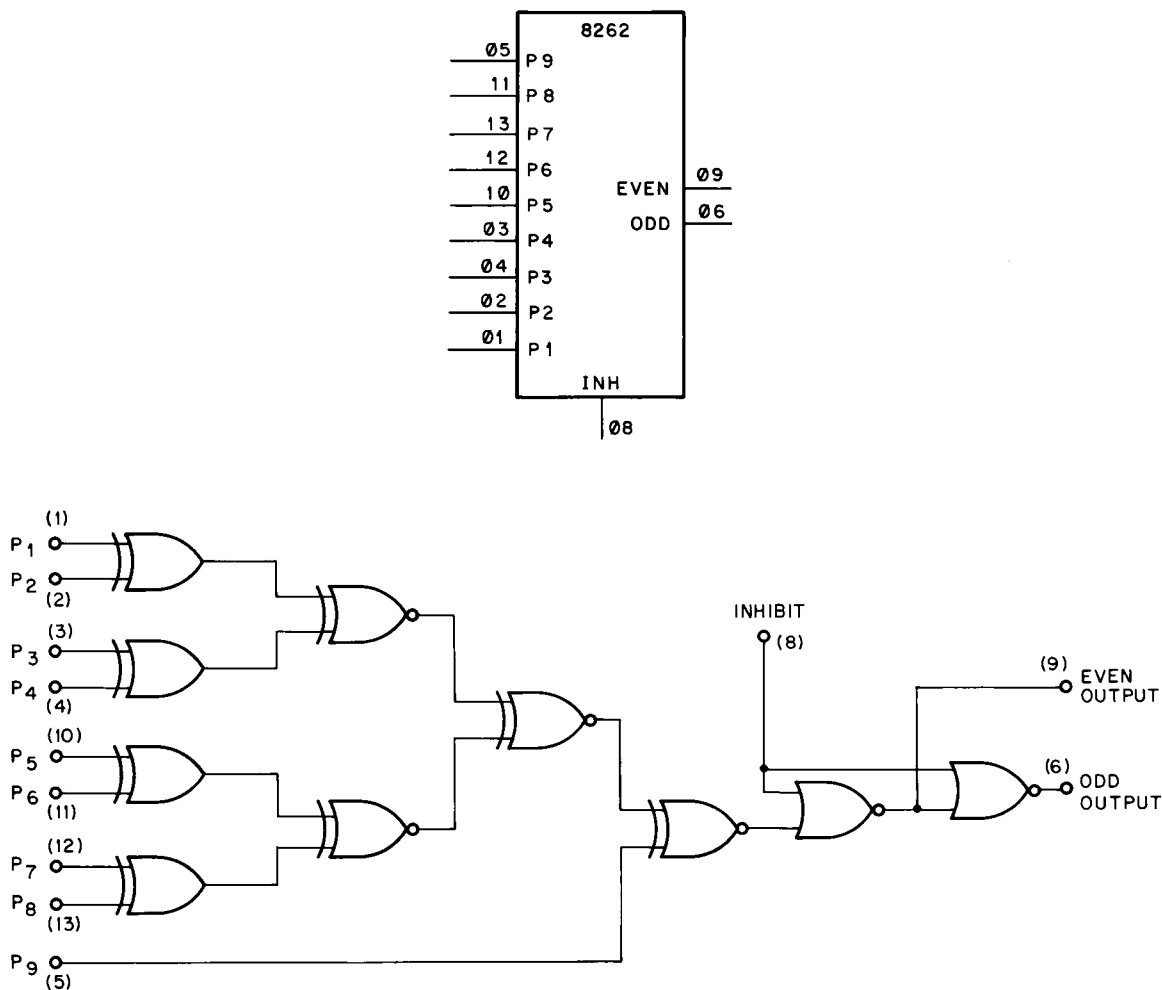
TRUTH TABLE

INPUTS						OUTPUTS	
A	B	G _Y	G _Z	S _A	S _B	Y	Z
X	X	L	X	X	X	H	$\bar{G}_Z$
H	X	X	X	H	X	H	$\bar{G}_Z$
X	H	X	X	X	H	H	$\bar{G}_Z$
L	L	H	X	X	X	L	H
L	X	H	X	X	L	L	H
X	L	H	X	L	X	L	H
X	X	H	X	L	L	L	H
X	X	X	L	X	X	X	H

IC-7520

82S62 9-BIT PARITY GENERATOR AND CHECKER

The 82S62 is a high-speed (Schottky) version of the 8262. The 82S62 Parity Generator/Checker has two outputs (EVEN and ODD) and an INHIBIT input that disables both outputs. A logic 1 on the INHIBIT input forces both outputs to logic 0. When used as a parity generator, the 82S62 supplies a parity bit which is transmitted with the data word. At the receiving end, the 82S62 can be used as a parity checker to indicate that data has been received correctly, or that an error has been detected.



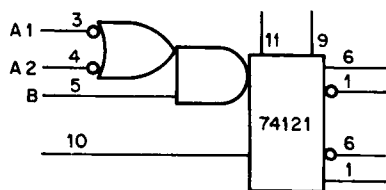
NOTES:

1. $V_{CC} = (14)$
2. $GND = (7)$
3. () = denotes pin number, pin numbers shown for Dual in-line package only
4. ODD OUTPUT = $P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9$
5. EVEN OUTPUT = $\overline{P_1 \oplus P_2 \oplus P_3 \oplus P_4 \oplus P_5 \oplus P_6 \oplus P_7 \oplus P_8 \oplus P_9}$

IC-8262

74121 MONOSTABLE MULTIVIBRATOR

The 74121 Monostable Multivibrator features dc triggering from positive or gated negative-going inputs. Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Once fired, the outputs are independent of the input pulses and are dependent only on the timing components on the chip. Input pulses may be of any duration relative to the output pulse.



TRUTH TABLE

t_n INPUT			t_{n+1} INPUT			OUTPUT
A1	A2	B	A1	A2	B	
1	1	0	1	1	1	INHIBIT
0	X	1	0	X	0	INHIBIT
X	1	0	X	0	0	INHIBIT
0	X	0	0	X	1	ONE SHOT
X	0	0	X	0	1	ONE SHOT
1	1	1	X	0	1	ONE SHOT
1	1	1	0	X	1	ONE SHOT
X	0	0	X	1	0	INHIBIT
0	X	0	1	X	0	INHIBIT
X	0	1	1	1	1	INHIBIT
0	X	1	1	1	1	INHIBIT
1	1	0	X	0	0	INHIBIT
1	1	0	0	X	0	INHIBIT

1 = $V_{in(1)} \geq 2 \text{ V}$

0 = $V_{in(0)} \leq 0.8 \text{ V}$

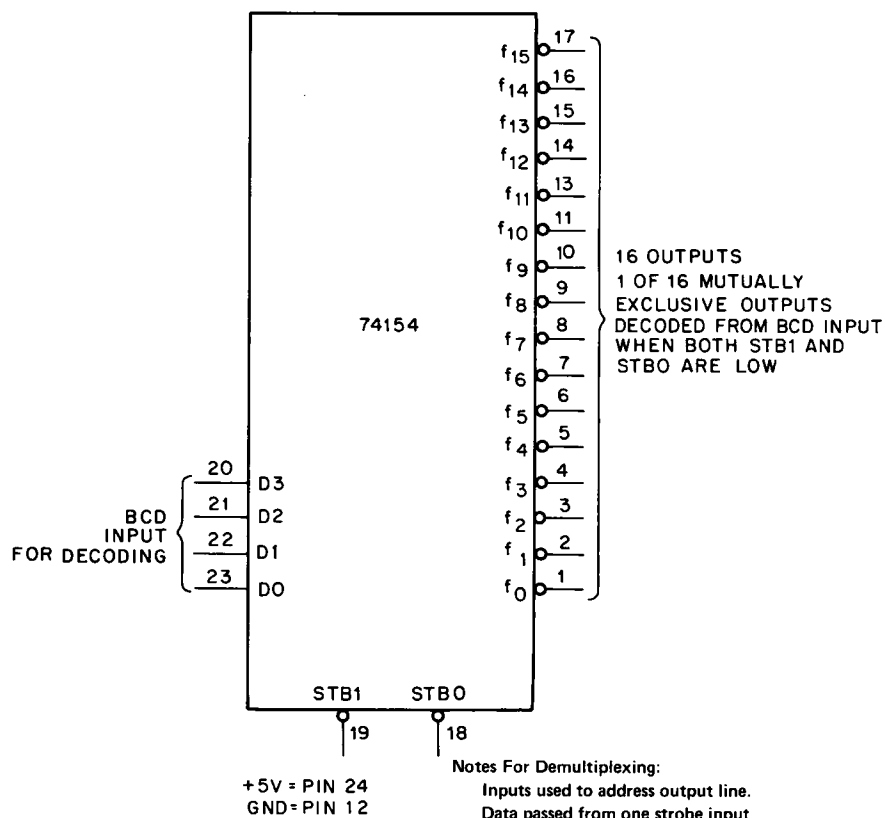
Note:

1. A1 and A2 are negative-edge-triggered logic inputs, and will trigger the one shot when either or both go to logical 0 with B at logical 1.
2. B is a positive Schmitt-trigger input for slow edges or level detection, and will trigger the one shot when B goes to logical 1 with either A1 or A2 at logical 0. (See Truth Table.)
3. Pins 9, 10, and 11 are inputs to control pulse width of output.

IC-74121

74154 4-LINE TO 16-LINE DECODER

The 74154 4-Line to 16-Line Decoder decodes four binary-coded inputs into one of 16 mutually-exclusive outputs when both strobe inputs (G1 and G2) are low. The decoding function is performed by using the four input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.



IC-74154



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MF11-W/WP CORE MEMORY SYSTEM
MAINTENANCE MANUAL
EK-MF11W-MM-001

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